CR-1

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
		?		?	?

Page	Circuits	ENG	Block
1	Table of Contents	KG	
2	Block Diagram	KG	
3	Microprocessor	KG	Processor
4	L3 CACHE & BYPASS	KG	
5	PANGEA PROCESSOR IF	KG	
6	PANGEA SDRAM IF & SDRAM DIMMS	KG	Sys Memory
7	SYSTEM CLOCKS, TERMS, CKE LATCH	KG	Clocks
8	PANGEA AGP INTERFACE, SYSTEM ROM	KG,LL	AGP, Graphics & ROM
9	VIDEO ASIC SEC 1 (AGP & VIDEO OUT)	LL	
10	VIDEO ASIC SEC 2 (FRAME BUFFER IF)	LL	
11	GRAPHICS SDRAMS	LL	
12	VIDEO ASIC SEC 3 (UNUSED CRUD!)	LL	
13	PANGEA ETHERNET, FIREWIRE, PWR/GNDS	RM	Enet, FW
14	PANGEA BYPASS	KG	
15	Ethernet PHY	RM	
16	Firewire PHY, Termination	LL	
17	PANGEA ATA, & PCMCIA BUSSES	RM	HD,Cdbus Modem,USB
18	PANGEA SER/AUD/USB, BOOTSTRAP PINS	RM	
19	USB CONN & PWR	RM	
20	MLB Pull-ups	ALL	PUs
21	L3 VOLTAGE REGULATORS, BOOTBANGER	KK	Power
22	Voltage Regulators	KK	
23	Power Manager Unit	KK	
24	ESP, LA CONNECTORS, AND CPU BYPASS	KG	CONNECTORS
25	Internal & External Video Conns	LL	
26	HD/CD/MODEM/PCMCIA/KITCHENSINK CONN'S	RM	
27	DC/DC CONVERTER (5V AND 3.3V)	KK	POWER STUFF
28	MORE POWER SUPPLY STUFF	KK	
29	TUMBLER AUDIO, CONTROL & D/A	LH	Audio
30	TUMBLER AUDIO, HEADPHONE DRIVER	LH	
31	TUMBLER AUDIO, INTERNAL MIC AND CALL PROGRESS	LH	
32	TUMBLER AUDIO, POWER AMPLIFIER	LH	
33	HOLES AND SLOTS, AND EMC TABLES	KG	
34-40	CONSTRAINT TABLES	ALL	
41-44	Part Tables	RM	

PVT

OCT 13, 2001

POWER RAIL DEFINITIONS

	RUN	SLEEP	SHUTDOWN
+5V	ON	ON	OFF
+5VSD	ON	OFF	OFF
+12V_MAIN	ON	ON	ON
+12VSD	ON	OFF	OFF
+3.3V	ON	ON	OFF

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

Apple Computer Inc.

TITLE
SCHEM,PCBA,"Clior"

DRAWING NUMBER 051-6101 REV. 12

SHT 1 OF 44

CORE SCHEMATIC PAGES

SDRAM DIMM 1 P. 6

SO-DIMM 0 P. 6

SYSTEM CLOCKS & SCHMOO P. 21

PANGEA BYPASS P. 14

L3 CACHE P. 4

LA CONN P. 24

TERM

MODEM CONN P. 26

CPU G3/G4 P. 3

(PT. 1) CPU IF P. 5

SDRAM IF P. 6 (PT. 2)

PANGEA (PT. 4) P. 13

FW IF ENET IF

(PT. 3) P. 8 AGP

SER (PT. 6)

USB

USB PORTS (4 PORTS) P. 19

(PT. 5) P. 17 UATA

P. 18 AUD

EDIE/CardBus

AUDIO CODEC/DAC P. 29

HEAD-PHONE JACK P. 30

MIC AMPS P. 31

FILTERS & EXT SPKR CONN P. 32

ESP CONN 20 PIN P. 24

PULL-UPS P. 20

FW PHY P.16

ENET PHY 10/100 MHZ P. 15

ROM 1M X 8 P. 8

GRAPHICS VIDEO CHIP GETS BIGGER EVERY DAY! P. 9,10,12

GRAPHICS SDRAM P. 11

VOLT REGS P. 22

POWER CONN, FP LED SWITCHES P. 27

PMU P. 23

DC/DC 5V AND 3.3V P. 27

EVT. VIDEO P. 25

INT/EXT VID CONNS P. 25

UATA CONN P. 26

CDBUS CONN P. 26 (WIRELESS)

LOCAL SCHEMATIC PAGES

Block Diagram

APPLE COMPUTER INC.

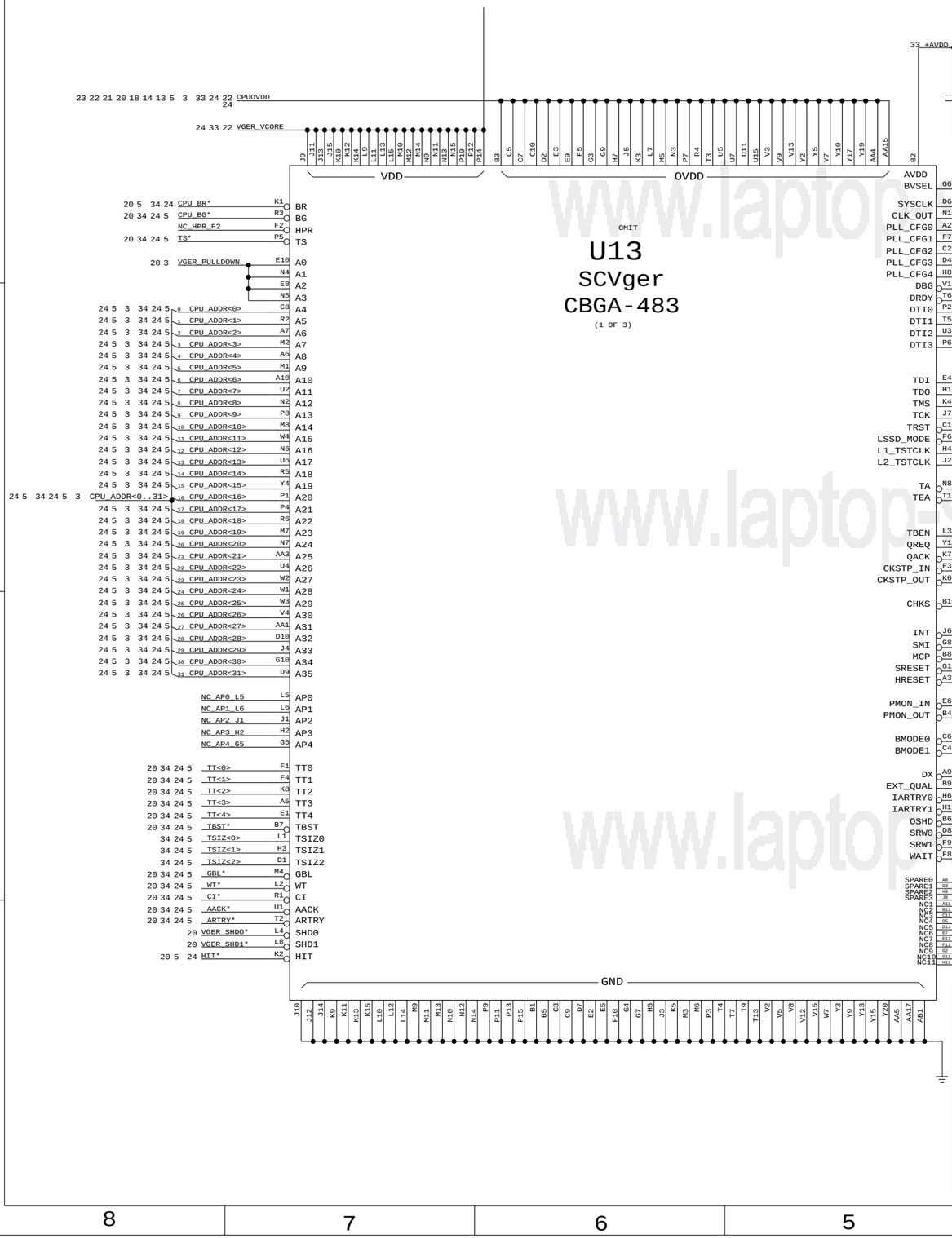
SIZE	DRAWING NUMBER	REV.
D	051-6101	12

SCALE: NONE

SHT 2 OF 44

CR-3

PRIORITY NETS ARE TS*, QREQ*, ARTRY*, BR*



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
110S1004	2	RES,10K-OHM,1%,1/16W	R249,R251		650_CPU_SPEED
110S1003	3	RES,1K-OHM,1%,1/16W	R267,R263,R265		650_CPU_SPEED
337T0071	1	MOT,SCVGER,V2.04+,733MHZ	U13	PROJECT	650_CPU_SPEED
110S1004	1	RES,10K-OHM,1%,1/16W	R250		700_CPU_SPEED
110S1003	4	RES,1K-OHM,1%,1/16W	R267,R263,R264,R266		700_CPU_SPEED
337S2861	1	IC,VGER,NODE 3,2.1,700MHZ,1.6VCORE,85C	U13	PROJECT	OMIT
337S2872	1	IC,VGER,NODE 3,2.2,700MHZ,1.65VCORE,85C	U13	PROJECT	700_CPU_SPEED
110S1004	2	RES,10K-OHM,1%,1/16W	R248,R249		800_CPU_SPEED
110S1003	3	RES,1K-OHM,1%,1/16W	R267,R265,R266		800_CPU_SPEED
337T0068	1	IC,VGER,NODE 3,2.1,800MHZ,1.6VCORE,85C	U13	PROJECT	OMIT
337S3016	1	IC,VGER,NODE 3,2.2,800MHZ,1.6VCORE,85C	U13	PROJECT	800_CPU_SPEED

Microprocessor

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6101	12
SCALE: NONE	SHT 3 OF 44	

CR-4

U13
SCVger
CBGA-483
(3 OF 3)

L30VDD

VGER_L3A<0>	L18	L3A0
VGER_L3A<1>	K22	L3A1
VGER_L3A<2>	L16	L3A2
VGER_L3A<3>	K20	L3A3
VGER_L3A<4>	K18	L3A4
VGER_L3A<5>	J22	L3A5
VGER_L3A<6>	J20	L3A6
VGER_L3A<7>	H22	L3A7
VGER_L3A<8>	J18	L3A8
VGER_L3A<9>	K16	L3A9
VGER_L3A<10>	H20	L3A10
VGER_L3A<11>	G22	L3A11
VGER_L3A<12>	F22	L3A12
VGER_L3A<13>	G20	L3A13
VGER_L3A<14>	H18	L3A14
VGER_L3A<15>	E22	L3A15
VGER_L3A<16>	J16	L3A16
VGER_L3A<17>	F20	L3A17

VGER_L3D<0>	AA19	L3D0
VGER_L3D<1>	AB20	L3D1
VGER_L3D<2>	U16	L3D2
VGER_L3D<3>	W18	L3D3
VGER_L3D<4>	AA20	L3D4
VGER_L3D<5>	AB21	L3D5
VGER_L3D<6>	AA21	L3D6
VGER_L3D<7>	T16	L3D7
VGER_L3D<8>	W20	L3D8
VGER_L3D<9>	U18	L3D9
VGER_L3D<10>	Y22	L3D10
VGER_L3D<11>	R16	L3D11
VGER_L3D<12>	V20	L3D12
VGER_L3D<13>	W22	L3D13
VGER_L3D<14>	T18	L3D14
VGER_L3D<15>	U20	L3D15
VGER_L3D<16>	N18	L3D16
VGER_L3D<17>	N20	L3D17
VGER_L3D<18>	N16	L3D18
VGER_L3D<19>	N22	L3D19
VGER_L3D<20>	M16	L3D20
VGER_L3D<21>	M18	L3D21
VGER_L3D<22>	M20	L3D22
VGER_L3D<23>	M22	L3D23
VGER_L3D<24>	R18	L3D24
VGER_L3D<25>	T20	L3D25
VGER_L3D<26>	U22	L3D26
VGER_L3D<27>	T22	L3D27
VGER_L3D<28>	R20	L3D28
VGER_L3D<29>	P18	L3D29
VGER_L3D<30>	R22	L3D30
VGER_L3D<31>	M15	L3D31
VGER_L3D<32>	G18	L3D32
VGER_L3D<33>	D22	L3D33
VGER_L3D<34>	E20	L3D34
VGER_L3D<35>	H16	L3D35
VGER_L3D<36>	C22	L3D36
VGER_L3D<37>	F18	L3D37
VGER_L3D<38>	D20	L3D38
VGER_L3D<39>	B22	L3D39
VGER_L3D<40>	G16	L3D40
VGER_L3D<41>	A21	L3D41
VGER_L3D<42>	G15	L3D42
VGER_L3D<43>	E17	L3D43
VGER_L3D<44>	A20	L3D44
VGER_L3D<45>	C19	L3D45
VGER_L3D<46>	C18	L3D46
VGER_L3D<47>	A19	L3D47
VGER_L3D<48>	A18	L3D48
VGER_L3D<49>	G14	L3D49
VGER_L3D<50>	E15	L3D50
VGER_L3D<51>	C16	L3D51
VGER_L3D<52>	A17	L3D52
VGER_L3D<53>	A16	L3D53
VGER_L3D<54>	C15	L3D54
VGER_L3D<55>	G13	L3D55
VGER_L3D<56>	C14	L3D56
VGER_L3D<57>	A14	L3D57
VGER_L3D<58>	E13	L3D58
VGER_L3D<59>	C13	L3D59
VGER_L3D<60>	G12	L3D60
VGER_L3D<61>	A13	L3D61
VGER_L3D<62>	E12	L3D62
VGER_L3D<63>	C12	L3D63

NC_L3DP0	AB19	NO_TEST	L3DP0
NC_L3DP1	AA22	NO_TEST	L3DP1
NC_L3DP2	P22	NO_TEST	L3DP2
NC_L3DP3	P16	NO_TEST	L3DP3
NC_L3DP4	C20	NO_TEST	L3DP4
NC_L3DP5	E16	NO_TEST	L3DP5
NC_L3DP6	A15	NO_TEST	L3DP6
NC_L3DP7	A12	NO_TEST	L3DP7

GND

L3VSEL — A4 VGER_L3VSEL — 20

L3CLK0 — V22 VGER_L3CLK<0> — 40 4
L3CLK1 — C17 VGER_L3CLK<1> — 40 4

L3CNTL0* — L20 VGER_L3CE* — 40 4
L3CNTL1* — L22 VGER_L3WE* — 40 4

L3ECHO_CLK0	V18	VGER_L3ECLK<0> 4 40
L3ECHO_CLK1	P20	VGER_L3ECLK<1> 4 40
L3ECHO_CLK2	E18	VGER_L3ECLK<2> 4 40
L3ECHO_CLK3	E14	40 4 VGER_L3ECLK<3>

NOL3_CACHE R728 10K 5% 1/16W MF 402
NOL3_CACHE R729 10K 5% 1/16W MF 402
NOL3_CACHE R730 10K 5% 1/16W MF 402
NOL3_CACHE R731 10K 5% 1/16W MF 402

4 33 21 L3_CORE

U14
TEMPLATE
SRAM_DDR_153PBGA
PBGA
OMIT

VDD VDDQ

VGER_L3A<0>	5T	A0
VGER_L3A<1>	5R	A1
VGER_L3A<2>	6R	A2
VGER_L3A<3>	4R	A3
VGER_L3A<2>	3T	A4
VGER_L3A<14>	3A	A5
VGER_L3A<9>	3C	A6
VGER_L3A<8>	4A	A7
VGER_L3A<11>	7C	A8
VGER_L3A<4>	4C	A9
VGER_L3A<10>	6C	A10
VGER_L3A<13>	6A	A11
VGER_L3A<7>	7P	A12
VGER_L3A<6>	7T	A13
VGER_L3A<12>	7A	A14
VGER_L3A<15>	3B	A15
VGER_L3A<16>	7B	A16
VGER_L3A<17>	7D	A17
L3_PULLDOWN	3D	A18
L3_PULLDOWN	3P	A19
VGER_L3CLK<0>	5G	CK
L3_VREF<1>	5H	CK*
L3_PULLDOWN	5C	G*
L3_PULLDOWN	4L	LBO*
VGER_L3CE*	5B	B1*
VGER_L3WE*	5K	B2*
L3_VREF<0>	5E	VREF
	5N	VREF
L3_ZQ<0>	5A	ZQ
ASIC_TMS	3U	TMS
DDR1_TDI	4U	TDI
DDR2_TDI	6U	TDO
ASIC_TCK	5U	TCK

9T VGER_L3D<5>	D0	
8T VGER_L3D<1>	D1	
9P VGER_L3D<10>	D2	
8P VGER_L3D<6>	D3	
9M VGER_L3D<13>	D4	
9K VGER_L3D<26>	D5	
8K VGER_L3D<8>	D6	
7K VGER_L3D<12>	D7	
9B VGER_L3D<23>	D8	
8B VGER_L3D<22>	D9	
9D VGER_L3D<19>	D10	
8D VGER_L3D<17>	D11	
9F VGER_L3D<30>	D12	
9H VGER_L3D<27>	D13	
8H VGER_L3D<15>	D14	
7H VGER_L3D<25>	D15	
1B VGER_L3D<20>	D16	
2B VGER_L3D<21>	D17	
1D VGER_L3D<31>	D18	
2D VGER_L3D<16>	D19	
1F VGER_L3D<29>	D20	
1H VGER_L3D<24>	D21	
2H VGER_L3D<9>	D22	
3H VGER_L3D<28>	D23	
1T VGER_L3D<2>	D24	
2T VGER_L3D<0>	D25	
1P VGER_L3D<7>	D26	
2P VGER_L3D<4>	D27	
1M VGER_L3D<11>	D28	
1K VGER_L3D<18>	D29	
2K VGER_L3D<3>	D30	
3K VGER_L3D<14>	D31	
NC_DQPA_U3 NO_TEST	DQPA	
NC_DQPB_U3 NO_TEST	DQPB	
NC_DQPC_U3 NO_TEST	DQPC	
NC_DQPD_U3 NO_TEST	DQPD	
VGER_L3ECLK<0> 40 4	CQ	
NC_8M_U3 TESTPOINT	CQ*	
VGER_L3ECLK<1> 40 4	CQ	
NC_2M_U3 TESTPOINT	CQ*	
L3_DDR* 4 20	B3*	
L3_MODE 4 20	MODE	
NC_7U_U3 TESTPOINT	NC	

4 33 21 L3_CORE

U30
TEMPLATE
SRAM_DDR_153PBGA
PBGA
OMIT

VDD VDDQ

L3_OVDD 4 33 4 21 22 20

VGER_L3A<0>	5T	A0
VGER_L3A<1>	5R	A1
VGER_L3A<3>	6R	A2
VGER_L3A<5>	4R	A3
VGER_L3A<6>	3T	A4
VGER_L3A<12>	3A	A5
VGER_L3A<11>	3C	A6
VGER_L3A<13>	4A	A7
VGER_L3A<9>	7C	A8
VGER_L3A<10>	4C	A9
VGER_L3A<4>	6C	A10
VGER_L3A<8>	6A	A11
VGER_L3A<7>	7P	A12
VGER_L3A<2>	7T	A13
VGER_L3A<14>	7A	A14
VGER_L3A<15>	3B	A15
VGER_L3A<16>	7B	A16
VGER_L3A<17>	7D	A17
L3_PULLDOWN	3D	A18
L3_PULLDOWN	3P	A19
VGER_L3CLK<1>	5G	CK
L3_VREF<1>	5H	CK*
L3_PULLDOWN	5C	G*
L3_PULLDOWN	4L	LBO*
VGER_L3CE*	5B	B1*
VGER_L3WE*	5K	B2*
L3_VREF<0>	5E	VREF
	5N	VREF
L3_ZQ<1>	5A	ZQ
ASIC_TMS	3U	TMS
DDR2_TDI	4U	TDI
DDR2_TDO	6U	TDO
ASIC_TCK	5U	TCK

9T VGER_L3D<55>	D0	
8T VGER_L3D<42>	D1	
9P VGER_L3D<60>	D2	
8P VGER_L3D<49>	D3	
9M VGER_L3D<50>	D4	
9K VGER_L3D<62>	D5	
8K VGER_L3D<58>	D6	
7K VGER_L3D<45>	D7	
9B VGER_L3D<61>	D8	
8B VGER_L3D<53>	D9	
9D VGER_L3D<57>	D10	
8D VGER_L3D<54>	D11	
9F VGER_L3D<63>	D12	
9H VGER_L3D<59>	D13	
8H VGER_L3D<56>	D14	
7H VGER_L3D<52>	D15	
1B VGER_L3D<47>	D16	
2B VGER_L3D<48>	D17	
1D VGER_L3D<44>	D18	
2D VGER_L3D<46>	D19	
1F VGER_L3D<41>	D20	
1H VGER_L3D<39>	D21	
2H VGER_L3D<51>	D22	
3H VGER_L3D<40>	D23	
1T VGER_L3D<34>	D24	
2T VGER_L3D<32>	D25	
1P VGER_L3D<38>	D26	
2P VGER_L3D<37>	D27	
1M VGER_L3D<33>	D28	
1K VGER_L3D<36>	D29	
2K VGER_L3D<43>	D30	
3K VGER_L3D<35>	D31	
NC_DQPA_U5 NO_TEST	DQPA	
NC_DQPB_U5 NO_TEST	DQPB	
NC_DQPC_U5 NO_TEST	DQPC	
NC_DQPD_U5 NO_TEST	DQPD	
VGER_L3ECLK<2> 40 4	CQ	
NC_8M_U5 TESTPOINT	CQ*	
VGER_L3ECLK<3> 40 4	CQ	
NC_2M_U5 TESTPOINT	CQ*	
L3_DDR* 4 20	B3*	
L3_MODE 4 20	MODE	
NC_7U_U5 TESTPOINT	NC	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
333S0009	2	SRAM,DDR,256KX36,250MHZ,153PIN	U14,U30	L3_CACHE

22 21 20 4 33 4 L3_OVDD

C642 C694 C698 C695 C622 C683 C697
C227 C222 C205 C192 C226 C196 C223
C638 C691 C684 C620 C616 C193 C624
0.1UF 20% 10V CERM 402

22 21 20 4 33 4 L3_OVDD

C705 10UF N20P80% 10V CERM 1206
C231 10UF N20P80% 10V CERM 1206
C188 0.1UF N20P80% 10V CERM 603
C689 2.2UF N20P80% 10V CERM 805

20 4 40 L3_VREF<0>

C716 0.1UF 20% 10V CERM 402
C715 0.1UF 20% 10V CERM 402

20 4 40 L3_VREF<1>

C718 0.1UF 20% 10V CERM 402
C719 0.1UF 20% 10V CERM 402

4 33 21 L3_CORE

C195 C204 C228 C221 C623
C680 C690 C639 C619 C621
0.1UF 20% 10V CERM 402

4 33 21 L3_CORE

C189 10UF N20P80% 10V CERM 1206
C190 10UF N20P80% 10V CERM 1206
NOSTUFF C213 150UF 20% 6.3V TANT SMD
C225 2.2UF N20P80% 10V CERM 805

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6101	12
SCALE: NONE	SHT 4 OF 44	

CR-5

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0555	1	PANGEA	U6	PROJECT	OMIT
343S0194	1	PANGEA, 688 BALL PANGEA	U6	PROJECT	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
343S0557	343S0194		U6	700 BALL PANGEA

22 21 20 18 14 13 5 3 33 24 22 3 CPUOVDD
24 23

NOSTUFF
R564 10 5% 1/16W MF 603

+3.3V
R565 10 1% 1/10W MF 603

33 PANGEA_AVDD5
C577 1UF 10% 10V CERM 805
C586 0.01UF 5% 50V CERM 603

AJ5 AVDD5

24 5 34 24 5 3 CPU_DATA<0..63>

U6
PANGEA
(1 OF 6)
PBGA
OMIT

MAXBUS
INTERFACE

20 34 24 3 CPU_BR*	AP16	BR		
20 34 24 3 CPU_BG*	AH19	BG		
20 34 24 3 TS*	AN14	TS		
24 3 34 24 5 3 CPU_ADDR<0..31>				
0 CPU_ADDR<0>	AK23	A_0	D_0	AJ15
1 CPU_ADDR<1>	AP27	A_1	D_1	AK6
2 CPU_ADDR<2>	AP28	A_2	D_2	AJ9
3 CPU_ADDR<3>	AN26	A_3	D_3	AK14
4 CPU_ADDR<4>	AK24	A_4	D_4	AM6
5 CPU_ADDR<5>	AN24	A_5	D_5	AH12
6 CPU_ADDR<6>	AM26	A_6	D_6	AM11
7 CPU_ADDR<7>	AJ23	A_7	D_7	AN18
8 CPU_ADDR<8>	AM24	A_8	D_8	AM18
9 CPU_ADDR<9>	AH23	A_9	D_9	AJ16
10 CPU_ADDR<10>	AM23	A_10	D_10	AK8
11 CPU_ADDR<11>	AN23	A_11	D_11	AH16
12 CPU_ADDR<12>	AJ22	A_12	D_12	AH8
13 CPU_ADDR<13>	AN22	A_13	D_13	AM14
14 CPU_ADDR<14>	AP26	A_14	D_14	AP3
15 CPU_ADDR<15>	AP21	A_15	D_15	AJ10
16 CPU_ADDR<16>	AH22	A_16	D_16	AN4
17 CPU_ADDR<17>	AM21	A_17	D_17	AJ12
18 CPU_ADDR<18>	AJ21	A_18	D_18	AM9
19 CPU_ADDR<19>	AK20	A_19	D_19	AN13
20 CPU_ADDR<20>	AK21	A_20	D_20	AK12
21 CPU_ADDR<21>	AN25	A_21	D_21	AK15
22 CPU_ADDR<22>	AP24	A_22	D_22	AM12
23 CPU_ADDR<23>	AP25	A_23	D_23	AP4
24 CPU_ADDR<24>	AH20	A_24	D_24	AH13
25 CPU_ADDR<25>	AH21	A_25	D_25	AP5
26 CPU_ADDR<26>	AP23	A_26	D_26	AH15
27 CPU_ADDR<27>	AM20	A_27	D_27	AN5
28 CPU_ADDR<28>	AJ20	A_28	D_28	AN6
29 CPU_ADDR<29>	AN21	A_29	D_29	AP6
30 CPU_ADDR<30>	AJ19	A_30	D_30	AJ13
31 CPU_ADDR<31>	AP22	A_31	D_31	AM15
20 34 24 3 CI*	AJ25	CI	D_32	AJ17
20 34 24 3 GBL*	AP29	GBL	D_33	AN12
20 34 24 3 TBST*	AN28	TBST	D_34	AN19
34 24 3 TSIZ<0>	AP30	TSIZ_0	D_35	AN17
34 24 3 TSIZ<1>	AN29	TSIZ_1	D_36	AN11
34 24 3 TSIZ<2>	AH25	TSIZ_2	D_37	AH17
20 34 24 3 TT<0>	AK27	TT_0	D_38	AN10
20 34 24 3 TT<1>	AP31	TT_1	D_39	AK17
20 34 24 3 TT<2>	AN30	TT_2	D_40	AN9
20 34 24 3 TT<3>	AM29	TT_3	D_41	AP19
20 34 24 3 TT<4>	AH26	TT_4	D_42	AM17
20 34 24 3 WT*	AK26	WT	D_43	AM8
20 3 34 24 AACK*	AN20	AACK	D_44	AJ11
20 34 24 3 ARTRY*	AP14	ARTRY	D_45	AK18
20 24 3 HIT*	AN16	HIT	D_46	AH14
20 34 24 3 QREQ*	AN15	QREQ	D_47	AM5
3 34 24 QACK*	AJ26	QACK	D_48	AH11
5 PANGEA_SUS_REQ_IN*	AJ32	SUSPENDREQ	D_49	AK9
23 PANGEA_SUSP_ACK*	AJ33	SUSPENDACK	D_50	AJ8
7 5 36 CPUFBIN	AK5	CPU_FB_IN	D_51	AJ14
36 CPUFBOUT	AL2	CPU_FB_OUT	D_52	AK11
	AM34	STOPCPUCLK	D_53	AH9
	AM30	ACS_REF	D_54	AH10
	AM1	CPU_CLK	D_55	AP10
			D_56	AP12
			D_57	AP8
			D_58	AP9
			D_59	AP13
			D_60	AP11
			D_61	AN7
			D_62	AN8
			D_63	AP7
			DBG	AJ18 — CPU_DBG* 24 34 3 20
			DRDY	AP15 — DRDY* 3 24 20
			DTI_0	AH24 — DBWO* 24 34 3 20
			DTI_1	AM27 — DTI<1> 24 3
			DTI_2	AN27 — DTI<2> 24 3 DTI<1..2> CAN BE OPEN FOR A G3
			TA	AJ24 — TA* 24 34 3 20
			TEA	AP20 — TEA* 24 34 3 20

AVSS5
AG7

CPUOVDD 3 22 24 33 3 5 13 14 18 20 21 22 23 24

PULLUP == MPC750 (G3)

G3 R579 4.75K 1% 1/16W MF 603

5 34 24 63 5 3 CPU_DATA<63>

G4 R578 4.75K 1% 1/16W MF 603

PULLDOWN == MAXBUS (G4)

ROUTE DELAY NETWORK ON INTERNAL LAYER

36 CPUFB4 — R246 0 — SHORT STUBS — 36 CPUFB3 — R245 0 — SHORT STUBS — 36 CPUFB2 — R234 0 — SHORT STUBS — 36 CPUFB1 — R223 0 — SHORT STUBS — 7 5 36 CPUFBIN

C589 20pF 10% 50V CERM 603 NOSTUFF

R256 0 NOSTUFF
R237 0 NOSTUFF
R225 0
R215 0 NOSTUFF

36 CPUFB5 — R247 0 — SHORT STUBS — 36 CPUFB6 — R244 0 — SHORT STUBS — 36 CPUFB7 — R233 0 NOSTUFF — SHORT STUBS — R222 0 — SHORT STUBS — TCPUFBOUT — R562 22 NOSTUFF — 36 CPUFBOUT

MAX-BUS"
(zero delay)

7 5 36 7 5 36 TCPUFBOUT

+3.3V
R182 10K 1% 1/16W MF 603 NOSTUFF

23 PANGEA_SUSP_REQ* — R174 0 — 5 PANGEA_SUS_REQ_IN*

+3.3V
R192 10K 1% 1/16W MF 603 NOSTUFF

7 23 CPU_STOP_CLK* — R189 0 — PANGEA_STOPCPUCLK

R570 1K 1% 1/16W MF 603 — PANGEA_ACS_REF

7 3 36 CPU_CLK — R566 22 NOSTUFF — 36 PANGEA_CPU_CLK

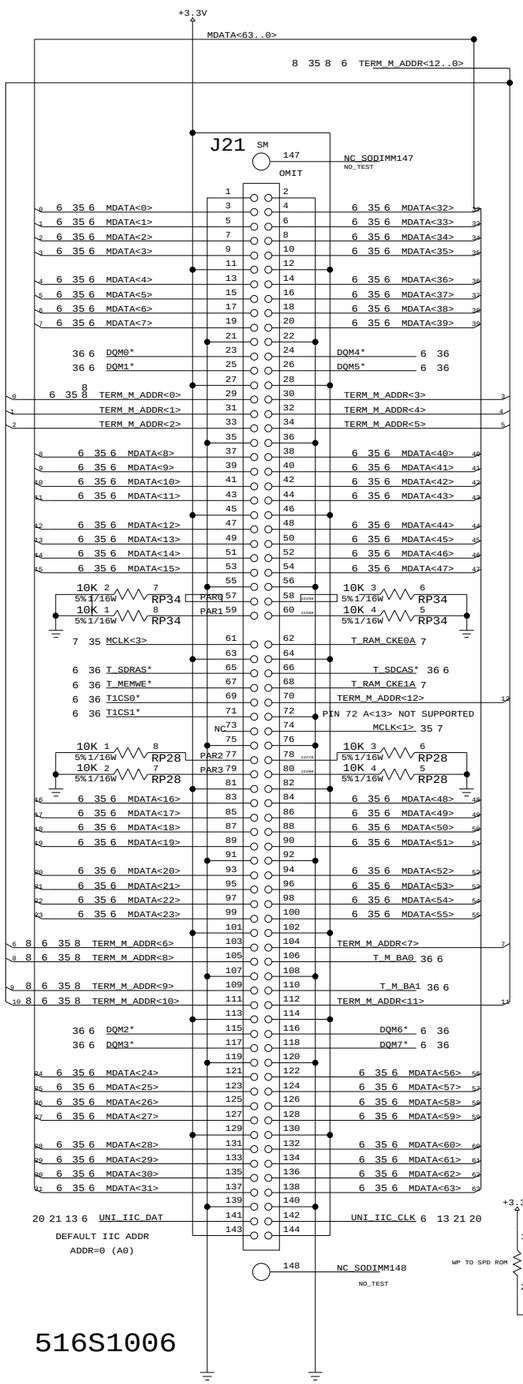
Series R on CPU_CLK work with shunt
R to drop voltage to 1.8V/2.5V

Pangea Processor IF

APPLE COMPUTER INC.

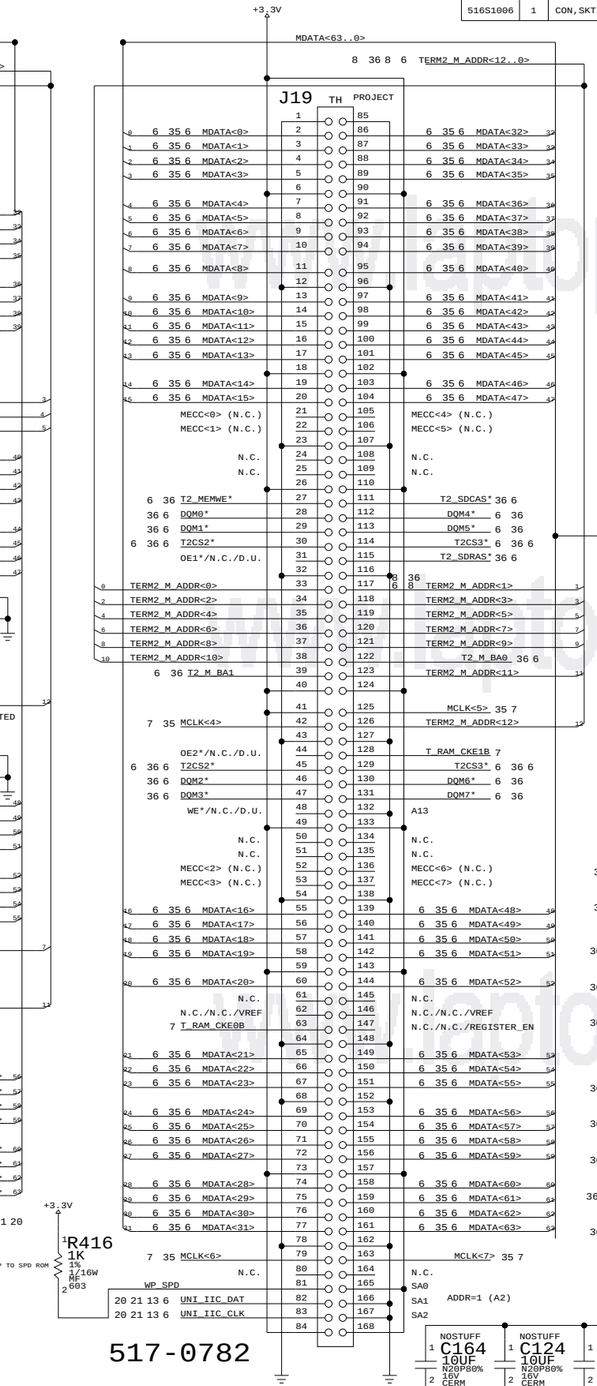
SIZE	DRAWING NUMBER	REV.
D	051-6101	12
SCALE: NONE	SHT 5 OF 44	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
516S1006	1	CON,SKT,SODIMM,SDRAM,3.3V,144P,BLK	J21	PROJECT	



516S1006

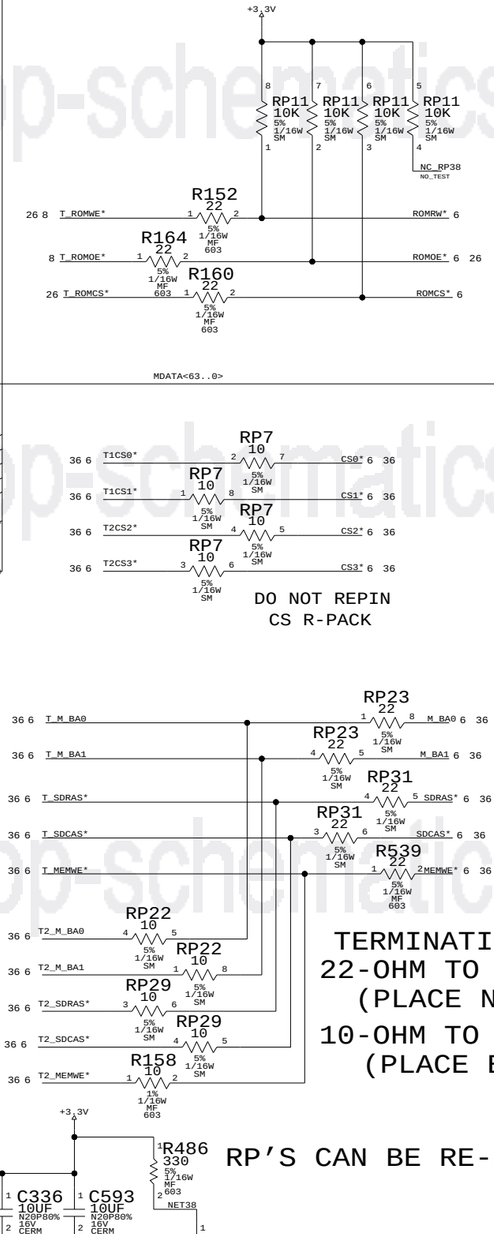
SO-DIMM A
FIRST DIMM



517-0782

PC100 DIMM B
SECOND DIMM

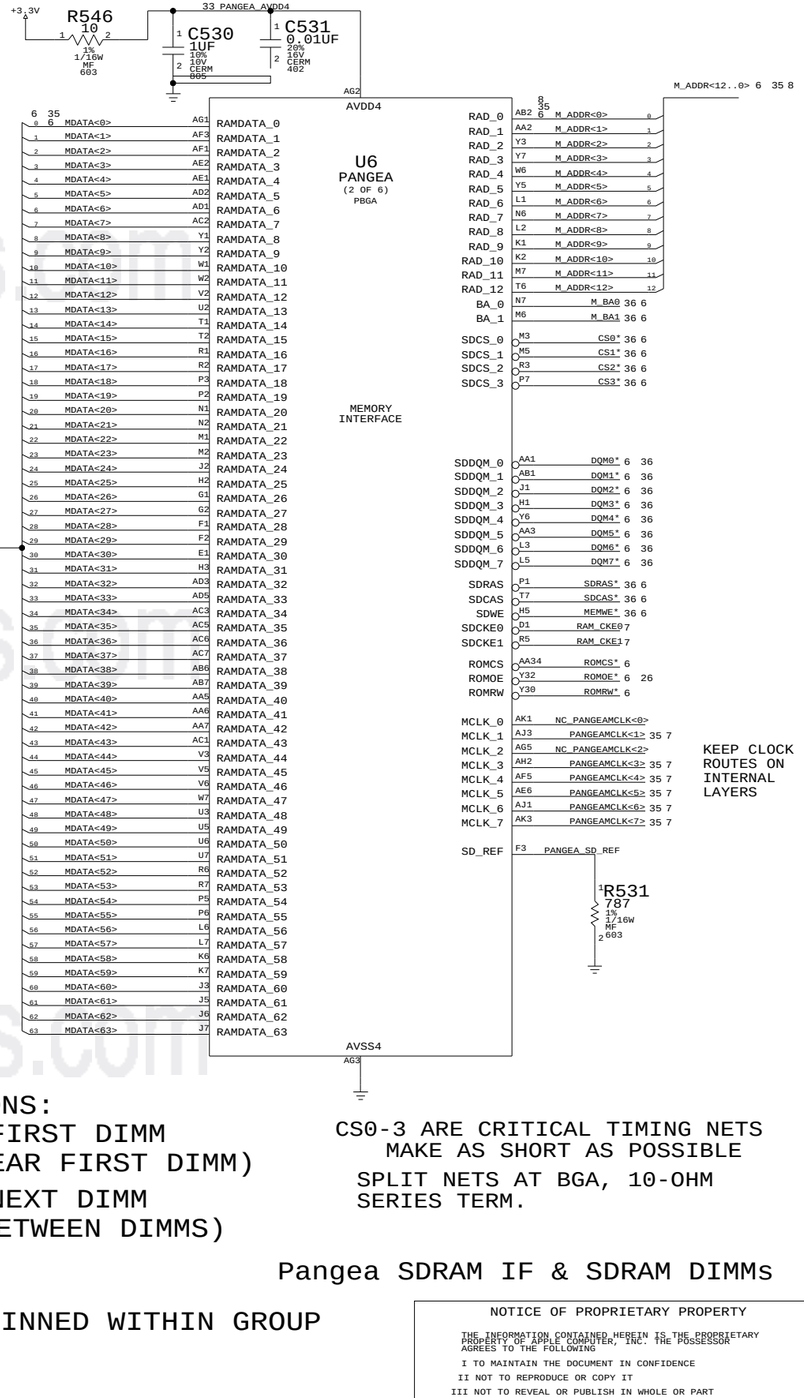
TERMINATIONS:
22-OHM TO FIRST DIMM
10-OHM TO NEXT DIMM



TERMINATIONS:
22-OHM TO FIRST DIMM
(PLACE NEAR FIRST DIMM)
10-OHM TO NEXT DIMM
(PLACE BETWEEN DIMMS)

RP’S CAN BE RE-PINNED WITHIN GROUP

STUFF BRIGHTER RED INSTEAD OF GREEN



KEEP CLOCK ROUTES ON INTERNAL LAYERS

CS0-3 ARE CRITICAL TIMING NETS
MAKE AS SHORT AS POSSIBLE

SPLIT NETS AT BGA, 10-OHM SERIES TERM.

Pangea SDRAM IF & SDRAM DIMMs

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6101	12
SCALE: NONE	SHT 6 OF 44	

PLACE NEAR PINS 1,7,16,21,23,29 ON SAME SIDE AS U33

PLACE 2.2UFS, ONE ON EITHER SIDE OF U33

C727 0.1UF 20% 10V CERM 402 (MEM_SS)
C729 0.1UF 20% 10V CERM 402 (MEM_SS)
C732 0.1UF 20% 10V CERM 402 (MEM_SS)
C734 0.1UF 20% 10V CERM 402 (MEM_SS)
C736 0.1UF 20% 10V CERM 402 (MEM_SS)
C738 0.1UF 20% 10V CERM 402 (MEM_SS)
C739 2.2UF N20P80% 16V CERM 805 (MEM_SS)
C741 10UF N20P80% 16V CERM 1206 (NOSTUFF)

C728 0.1UF 20% 10V CERM 402 (MEM_SS)
C730 0.1UF 20% 10V CERM 402 (MEM_SS)
C733 0.1UF 20% 10V CERM 402 (MEM_SS)
C735 0.1UF 20% 10V CERM 402 (MEM_SS)
C737 0.1UF 20% 10V CERM 402 (MEM_SS)
C740 2.2UF N20P80% 16V CERM 805 (MEM_SS)

PLACE NEAR PINS 35, 41, 47, 52, 56 ON SAME SIDE AS U33

+3.3V

L68 1000-OHM-EMI SM (MEM_SS)
L69 1000-OHM-EMI SM (MEM_SS)
C725 0.1UF 20% 10V CERM 402 (MEM_SS)

7 33 MAINCLK_VDD

R654 10K 5% 1/16W MF 402 (MEM_SS)
R667 10K 5% 1/16W MF 402 (NOSTUFF)

R625 100K 1% 1/16W MF 603 (MEM_SS)
R628 100K 1% 1/16W MF 603 (MEM_SS)
R636 100K 1% 1/16W MF 603 (MEM_SS)

R627 470 1% 1/16W MF 603 (NOSTUFF)
R635 470 1% 1/16W MF 603 (NOSTUFF)
R637 470 1% 1/16W MF 603 (NOSTUFF)

0 0 0 = TRISTATE
0 1 0 = 66 MHZ
1 1 1 = 100 MHZ
0 1 1 = 125 MHZ
1 1 0 = 133 MHZ
0 0 1 = 140 MHZ
1 0 1 = 150 MHZ

CPU_STOP_OE

MAINCLK_FS0
MAINCLK_FS1
MAINCLK_FS2

R638 0 5% 1/16W MF 603 (MEM_SS) — 5 23 CPU_STOP_CLK*

R652 470 1% 1/16W MF 603 (NOSTUFF)

J26 U.FL-R SMT F-ST-SM (NOSTUFF) — 518S0104

R761 0 5% 1/16W MF 603 (NOSTUFF) — FMAX_SS_XIN / SS_XIN

R762 49.9 1% 1/16W MF 603 (NOSTUFF)

R761.2 AND R763.1 TO SHARE PAD.

R763 0 5% 1/16W MF 603

LOCATE NEAR PANGEA

CAN BE RE-PINNED

+3.3V

C401 0.1UF N20P80% 16V CERM 603 (PROJECT)

U9 74LVT574 TSSOP
VCC, GND
D1 D2 D3 D4 D5 D6 D7 D8
Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8
CLK, OE

R532 22 1/16W 5% MF 603 — 6 RAM_CKE0 — T_RAM_CKE0
R541 22 1/16W 5% MF 603 — 6 RAM_CKE1 — T_RAM_CKE1

RP35 22 5% 1/16W SM
T_RAM_CKE0A 6
T_RAM_CKE0B 6
T_RAM_CKE1A 6
T_RAM_CKE1B 6

5 36 CPUFBIN

CPUFBIN SHOULD BE VERY SHORT
FROM PANGEA INPUT PIN TO CKE BUFFER

U33 C5003 SSOI PROJECT MEM_SS

VDD: 1 7 16 21 23 29 35 41 47 52 56
VSS: 4 8 22 26 32 38 44 48 53

FSEL0 18
FSEL1 19
FSEL2 20

DLA0 9 — NO_TEST NC_MAINCLK_DLA0
DLA1 10 — NO_TEST NC_MAINCLK_DLA1
DLA2 11 — NO_TEST NC_MAINCLK_DLA2
DLA3 12 — NO_TEST NC_MAINCLK_DLA3
DLA4 13 — NO_TEST NC_MAINCLK_DLA4
DLA5 14 — NO_TEST NC_MAINCLK_DLA5
DLA6 15 — MAINCLK_DLA6

CPU0 55 — NO_TEST NC_CPU0
CPU1 54
CPU2 51 — NC_CPU2 NO_TEST
CPU3 50 — NC_CPU3 NO_TEST
CPU4 49 — NC_CPU4 NO_TEST

DLB0/SDRAM0 46
DLB1/SDRAM1 45
DLB2/SDRAM2 43
DLB3/SDRAM3 42
DLB4/SDRAM4 40
DLB5/SDRAM5 39
DLB6/SDRAM6 37

DLC0/SDRAM7 36
DLC1/SDRAM8 34 — SDRAM7 — NC_SDRAM8 NO_TEST
DLC2/SDRAM9 33 — NC_SDRAM9 NO_TEST
DLC3/SDRAM10 31
DLC4/SDRAM11 30
DLC5/SDRDCLK 28
DLC6 27

OE 17 — CPU_STOP_OE
REF0 2 — TEST POINT NC_REF0
REF1 3 — TEST POINT NC_REF1
SCLK 24 — 20 23 PMU_IIC_CLK
SDATA 25 — 20 23 PMU_IIC_DAT
XIN 5 — SS_XIN
XOUT 6

Y8 14.318M SM (MEM_SS) — 35 MAINCLK_XIN / 35 MAINCLK_XOUT

R670 330K 5% 1/16W MF 603 (NOSTUFF)

C726 15PF 5% 50V CERM 603 (NOSTUFF)
C731 15PF 5% 50V CERM 603 (NOSTUFF)

R678 10 5% 1/16W MF 402 (DEVELOPMENT) — CPU1 — CPU_LA_CLK 24

R580 10 5% 1/16W MF 402 (MEM_SS) — 35 MCLKOUT<5> — MCLK<5> 6 35 7
R560 10 5% 1/16W MF 402 (MEM_SS) — 35 MCLKOUT<4> — MCLK<4> 6 35 7
R680 10 5% 1/16W MF 402 (MEM_SS) — 35 MCLKOUT<1> — MCLK<1> 6 35 7
R668 10 5% 1/16W MF 402 (MEM_SS) — 35 MCLKOUT<3> — MCLK<3> 6 35 7
R572 10 5% 1/16W MF 402 (MEM_SS) — 35 MCLKOUT<6> — MCLK<6> 6 35 7
R624 10 5% 1/16W MF 402 (MEM_SS) — MCLKOUT<9> — TCPUFBOUT 36 5

DLB6 7

R681 10 5% 1/16W MF 402 (DEVELOPMENT) — LACLK 26

R656 10 5% 1/16W MF 402 (MEM_SS) — 35 MCLKOUT<7> — MCLK<7> 6 35 7

R676 22 5% 1/16W MF 603 (MEM_SS) — MAIN_CPU_CLK 36 3 5 — CPU_CLK

SDRDCLKOUT

R548 10K 5% 1/16W MF 402 (MEM_SS) — MAINCLK_DLC6 7

R550 10 5% 1/16W MF 402 (NOSTUFF) — 35 6 PANGEAMCLK<1> — MCLK<1> 6 35 7
R556 10 5% 1/16W MF 402 (NOSTUFF) — 35 6 PANGEAMCLK<3> — MCLK<3> 6 35 7
R547 10 5% 1/16W MF 402 (NOSTUFF) — 35 6 PANGEAMCLK<4> — MCLK<4> 6 35 7
R543 10 5% 1/16W MF 402 (NOSTUFF) — 35 6 PANGEAMCLK<5> — MCLK<5> 6 35 7
R558 10 5% 1/16W MF 402 (NOSTUFF) — 35 6 PANGEAMCLK<6> — MCLK<6> 6 35 7
R552 10 5% 1/16W MF 402 (NOSTUFF) — 35 6 PANGEAMCLK<7> — MCLK<7> 6 35 7

33 7 MAINCLK_VDD

R653 10K 5% 1/16W MF 402 (MEM_SS) — DLB6 7
R657 10K 5% 1/16W MF 402 (MEM_SS) — MAINCLK_DLC6 7

SYSTEM CLOCKS, TERMS, CKE LATCH

THE FOLLOWING RESISTORS SHARE PADS

MCLK<1>	R550.2	R680.2
MCLK<3>	R556.2	R668.2
MCLK<4>	R547.2	R560.2
MCLK<5>	R543.2	R580.2
MCLK<6>	R558.2	R572.2
MCLK<7>	R552.2	R656.2
CPU_CLK	R676.2	R566.1 SHEET 5
TCPUFBOUT	R624.2	R562.1 SHEET 5

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6101 | REV. 12
SCALE NONE | SHT 7 OF 44

FLASH ROM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S0350	1	BOOT ROM, BLANK	U7	PROJECT	OMIT
341S1125	1	BOOT ROM, P11-4.2.1A10	U7	PROJECT	OMIT
341S1144	1	BOOT ROM, P11-4.2.5A2	U7	PROJECT	

+3.3V

C141 0.1UF N20P80% 603 CERM 16V

C142 0.1UF N20P80% 16V CERM 603

U7 FEPR-1MX8 110 TSOP OMIT

VPP VCC GND

A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16 A17 A18 A19 A20

DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7

IOADDR<0> IOADDR<1> IOADDR<2> IOADDR<3> IOADDR<4> IOADDR<5> IOADDR<6> IOADDR<7> IOADDR<8> IOADDR<9> IOADDR<10> IOADDR<11> IOADDR<12> IOADDR<13> IOADDR<14> IOADDR<15> IOADDR<16> IOADDR<17> IOADDR<18> IOADDR<19> IOADDR<20>

IODATA<7..0> 8 17 39 18 26

IODATA<0> IODATA<1> IODATA<2> IODATA<3> IODATA<4> IODATA<5> IODATA<6> IODATA<7>

ROM_ONBOARD_CS* T_ROMOE* T_ROMWE* UNI_RESET*

RESET FLASH AT RESTART

ENABLE WRITES TO BOOT BLOCK

R154 1K 1% 1/16W MF 603

BOOTWP*

R147 10K 1% 1/16W MF 603 NOSTUFF

DISABLE WRITES TO BOOT BLOCK

TERMINATIONS:
22-OHM TO FIRST DIMM (PLACE NEAR FIRST DIMM)
10-OHM TO NEXT DIMM (PLACE BETWEEN DIMMS)

M_ADDR<12..0> 8 35 6

TERM_M_ADDR<12..0> 6 35 6 8

TERM2_M_ADDR<12..0> 6 36 6 8

RP33 22 5% 1/16W SM 8 35 6

RP9 22 5% 1/16W SM 8 35 6

RP31 22 5% 1/16W SM 8 35 6

RP9 22 5% 1/16W SM 8 35 6

RP31 22 5% 1/16W SM 8 35 6

RP9 22 5% 1/16W SM 8 35 6

RP21 22 5% 1/16W SM 8 35 6

RP23 22 5% 1/16W SM 8 35 6

RP21 22 5% 1/16W SM 8 35 6

RP21 22 5% 1/16W SM 8 35 6

RP21 22 5% 1/16W SM 8 35 6

RP23 22 5% 1/16W SM 8 35 6

R540 22 5% 1/16W MF 603 8 35 6 1

RP29 10 5% 1/16W SM 8 6 36 8 6 8

RP29 10 5% 1/16W SM 8 6 36

RP26 10 5% 1/16W SM 8 6 36

RP26 10 5% 1/16W SM 8 6 36

RP26 10 5% 1/16W SM 8 6 36

RP24 10 5% 1/16W SM 8 6 36

RP24 10 5% 1/16W SM 8 6 36

RP24 10 5% 1/16W SM 8 6 36

RP22 10 5% 1/16W SM 8 6 36

RP22 10 5% 1/16W SM 8 6 36

R123 10 1% 1/16W MF 603 8 6 1 36

RP'S CAN BE RE-PINNED

+3.3V

R538 10 1% 1/16W MF 603

PLACE CLOSE TO EACH AGPVDD PIN

33 AGPVDD

C450 0.1UF 20% 10V CERM 402

C449 0.01UF 20% 16V CERM 402

R530 10 1% 1/16W MF 603

33 PANGEA_AVDD6

C448 1UF 10% 10V CERM 805

C458 0.01UF 20% 16V CERM 402

AGPVDD H7 H6

AVDD6 F5

STPAGP* AGPBUSY* WILL BE SUPPORTED in future AGP graphics controllers.

R498 4.99K 1% 1/16W MF 603

R516 0 5% 1/16W MF 603 NOSTUFF

20 9 AGPSTOP* PAN_AGPSTOP*

9 33 AGPVREF

R499 3.32K 1% 1/16W MF 603

C407 0.01UF 20% 16V CERM 402

C406 0.01UF 20% 16V CERM 402

C405 0.01UF 20% 16V CERM 402

PLACE CAPS NEAR PANGEA BALLS

VREF FOR AGP BUS = 1.32V

R515 10K 1% 1/16W MF 603

9 AGPBUSY* R514 0 5% 1/16W MF 603 NOSTUFF PAN_AGPBUSY*

9 37 AGP_CLK 37 R522 22 5% 1/16W MF 603 PANGEA_AGP_CLK

KEEP CLOCKS ON INTERNAL LAYERS

37 AGP_FB_IN AGP_FB_OUT

R523 22 5% 1/16W MF 603

SHORT STUBS R118 0 5% 1/16W MF 603 NOSTUFF 36 AGPFB3 R119 0 5% 1/16W MF 603 SHORT STUBS

R115 0 5% 1/16W MF 603

R117 0 5% 1/16W MF 603 NOSTUFF

36 AGPFB2 R114 0 5% 1/16W MF 603 NOSTUFF SHORT STUBS

36 AGPFB1 R116 0 5% 1/16W MF 603 SHORT STUBS

36 AGPFB0 SHORT STUBS

STP_AGP AGPPVT AGPVREF1 AGPVREF2 AGPVREF3 AGP_BUSY AGP_CLK AGP_FB_IN AGP_FB_OUT

U6 PANGEA (3 OF 6) PBGA

PCI/AGP INTERFACES

AGPREQ* AGPGNT*

AGPAD<31..0> 8 9 37 9

PCI0AD0 PCI0AD1 PCI0AD2 PCI0AD3 PCI0AD4 PCI0AD5 PCI0AD6 PCI0AD7 PCI0AD8 PCI0AD9 PCI0AD10 PCI0AD11 PCI0AD12 PCI0AD13 PCI0AD14 PCI0AD15 PCI0AD16 PCI0AD17 PCI0AD18 PCI0AD19 PCI0AD20 PCI0AD21 PCI0AD22 PCI0AD23 PCI0AD24 PCI0AD25 PCI0AD26 PCI0AD27 PCI0AD28 PCI0AD29 PCI0AD30 PCI0AD31

AGPCBE<3..0> 8 9 37 9

PCI0BE_0 PCI0BE_1 PCI0BE_2 PCI0BE_3

PCI0PAR PCI0FRAME PCI0TRDY PCI0IRDY PCI0STOP PCI0DEVSEL

SBA0 SBA1 SBA2 SBA3 SBA4 SBA5 SBA6 SBA7

SB_STB

ST0 ST1 ST2 AD_STB0 AD_STB1 PIPE RBF

R517 22 5% 1/16W MF 603 AGPADSTB<0> 37 9 20

R518 22 5% 1/16W MF 603 AGPADSTB<1> 37 9 20

AVSS6

Pangea AGP IF, System ROM

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6101 | REV. 12

SCALE NONE | SHT 8 OF 44

CR-9

GRAPHICS CONTROLLER - AGP AND VIDEO INTERFACES

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S0208	1	IC,MONICA GRAPHICS CTLR (A02)	U22	PROJECT	OMIT
338S0010	1	IC,MONICA GRAPHICS CTLR (B01)	U22	PROJECT	OMIT
338S0021	1	IC,MONICA GRAPHICS CTLR (B02)	U22	PROJECT	OMIT
338S0021	1	IC,MONICA GRAPHICS CTLR (B03)	U22	PROJECT	

The resistor to the left may be used instead of the regulator if there is a problem with resetting the TMDS xmtr in Monica.

R404 AND R386 MUST be placed close to each other and pin AK7 of Monica.

Match lengths and route on internal layers:
Nets INT_TMDS_XXX

<---- GPIODx
initial conditions

ROUTE THE RGB LINES AS 75 OHM TRACES.

All of the components to the right must be placed very close to the respective pins on the chip!

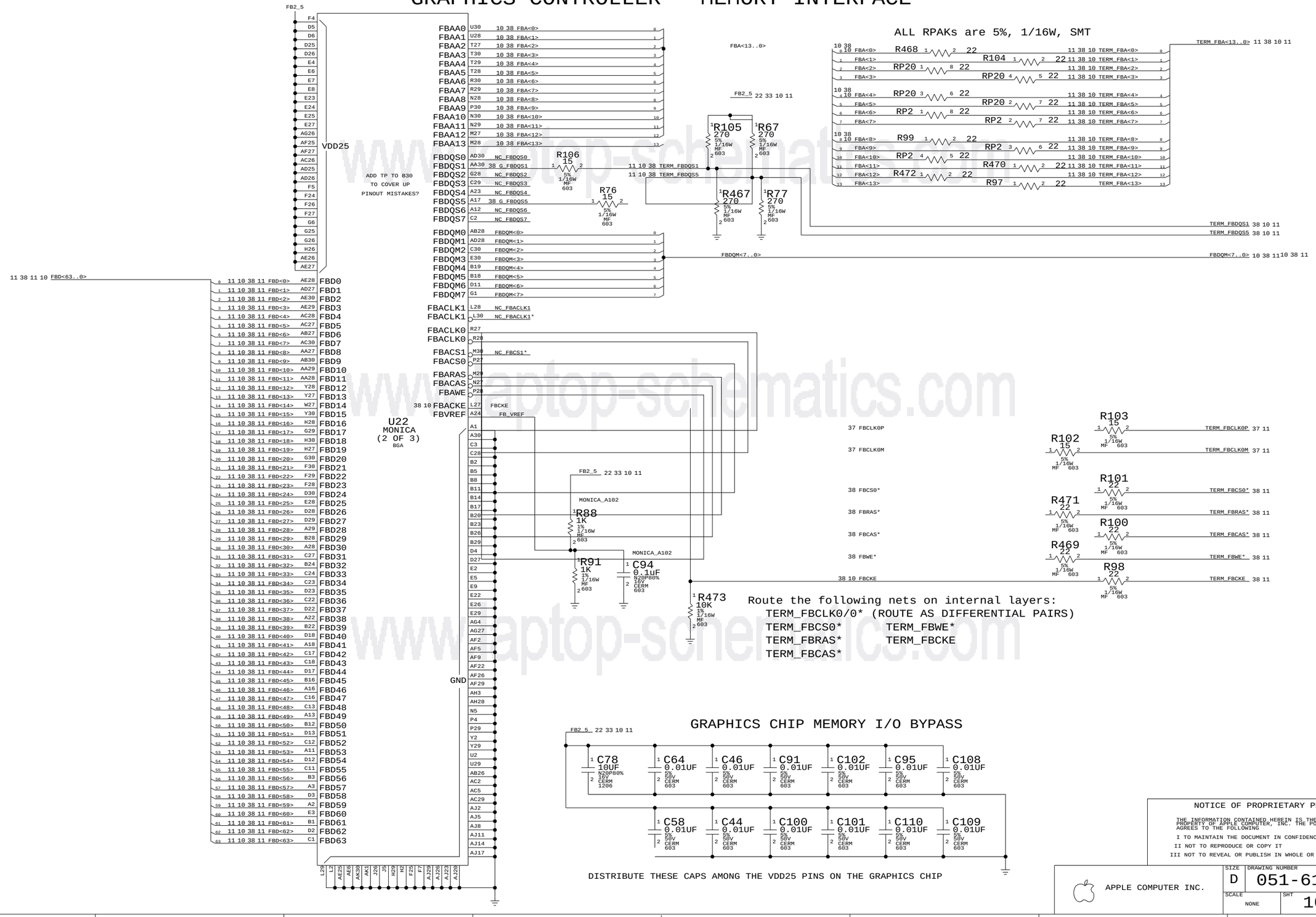
GRAPHICS CORE BYPASS (VDD)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6101	12
SCALE: NONE	SHT 9 OF 44	

CR-10

GRAPHICS CONTROLLER - MEMORY INTERFACE



APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6101	12
SCALE: NONE	SHT 10 OF 44	

CR-11

GRAPHICS SDRAMS - 16/32 MB

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
333S0055	333S0006	SAMSUNG_SGRAM	U3,U21	2MX32,2.5VCC,183MHZ

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333S0075	2	IC,SGRAM,DDR,2MX32,125MHZ,100P TQFP, NO DLL	U3,U21	PROJECT	OMIT
333S0076	2	IC,SGRAM,DDR,2MX32,143MHZ,100P TQFP, NO DLL	U3,U21	PROJECT	OMIT
333S0077	2	IC,SGRAM,DDR,2MX32,166MHZ,100P TQFP, NO DLL	U3,U21	PROJECT	OMIT
333S0003	2	IC,SDRAM,2MX32,DLL,143MHZ,100P TQFP (SAM)	U3,U21	PROJECT	OMIT
333S0004	2	IC,SDRAM,2MX32,DLL,166MHZ,100P TQFP (SAM)	U3,U21	PROJECT	OMIT
333S0005	2	IC,SDRAM,2MX32,2.5VCC,143MHZ,100P TQFP (M-H)	U3,U21	PROJECT	OMIT
333S0006	2	IC,SDRAM,2MX32,2.5VCC,166MHZ,100P TQFP (M)	U3,U21	PROJECT	M-H_SGRAM
333S0006	2	IC,SDRAM,2MX32,DLL,166MHZ,100P TQFP (SAM)	U3,U21	PROJECT	SAMSUNG_SGRAM

11 10 33 22 FB2_5

C330 10UF N20P80% 16V CERM 1206
C374 10UF N20P80% 16V CERM 1206
C352 0.01UF 5% 50V CERM 603
C348 0.01UF 5% 50V CERM 603
C343 0.01UF 5% 50V CERM 603
C340 0.01UF 5% 50V CERM 603

FB2_5

C113 10UF N20P80% 16V CERM 1206
C40 10UF N20P80% 16V CERM 1206
C37 0.01UF 5% 50V CERM 603
C42 0.01UF 5% 50V CERM 603
C63 0.01UF 5% 50V CERM 603
C99 0.01UF 5% 50V CERM 603
C333 0.01UF 5% 50V CERM 603
C98 0.01UF 5% 50V CERM 603
C367 0.01UF 5% 50V CERM 603
C328 0.01UF 5% 50V CERM 603

11 10 33 22 FB2_5

C73 10UF N20P80% 16V CERM 1206
C36 0.01UF 5% 50V CERM 603
C376 0.01UF 5% 50V CERM 603
C38 0.01UF 5% 50V CERM 603
C377 0.01UF 5% 50V CERM 603

FB2_5

C371 10UF N20P80% 16V CERM 1206
C39 10UF N20P80% 16V CERM 1206
C360 0.01UF 5% 50V CERM 603
C43 0.01UF 5% 50V CERM 603
C85 0.01UF 5% 50V CERM 603
C339 0.01UF 5% 50V CERM 603
C84 0.01UF 5% 50V CERM 603
C332 0.01UF 5% 50V CERM 603
C359 0.01UF 5% 50V CERM 603
C366 0.01UF 5% 50V CERM 603

10 38 11 10 FBD<63..0>
11 38 10 FBDQM<7..0>
11 10 38 11 10 TERM_FBA<13..0>

U3
SGRAM_2MX32
64MBIT
FLA
PROJECT
OMIT

FB2_5	VDD1	15	
	VDD2	35	
	VDD3	65	
	VDD4	96	
	VDDQ1	2	FB2_5
	VDDQ2	8	
	VDDQ3	14	
	VDDQ4	22	
	VDDQ5	59	
	VDDQ6	67	
	VDDQ7	73	
	VDDQ8	79	
	VDDQ9	86	
	VDDQ10	95	
11 10 38 TERM_FBA<0>	A0	31	
TERM_FBA<1>	A1	32	
TERM_FBA<2>	A2	33	
TERM_FBA<3>	A3	34	
TERM_FBA<4>	A4	47	
TERM_FBA<5>	A5	48	
TERM_FBA<6>	A6	49	
TERM_FBA<7>	A7	50	
TERM_FBA<8>	A8	51	
TERM_FBA<9>	A9	45	
TERM_FBA<10>	A10	36	
	CKE	53	
TERM_FBCLK0P	CK	55	
TERM_FBCLK0M	CK	54	
	CS	28	
	WE	25	
	CAS	26	
	RAS	27	
NO_TEST NC_SGRAM1RFU	RFU	93	
38 M_FBDQS1	DQS	94	
33 M_VREF1	VREF	58	
	DSF/MCL	52	
11 10 38 11 10 TERM_FBA<11>	BA0	29	
TERM_FBA<12>	BA1	30	
	VSSQ1	5	
	VSSQ2	11	
	VSSQ3	19	
	VSSQ4	62	
	VSSQ5	70	
	VSSQ6	76	
	VSSQ7	82	
	VSSQ8	92	
	VSSQ9	99	
	VSS1	16	
	VSS2	46	
	VSS3	66	
	VSS4	85	
	NC1	37	
	NC2	38	
	NC3	39	
	NC4	40	
	NC5	41	
	NC6	42	
	NC7	43	
	NC8	44	
	NC13	91	
	NC12	90	
	NC11	89	
	NC10	88	
	NC9	87	
	DM0	23	FBDQM<2> 2
	DM1	56	FBDQM<1> 1
	DM2	24	FBDQM<3> 3
	DM3	57	FBDQM<0> 0
	DQ0	97	FBD<16> 16
	DQ1	98	FBD<17> 17
	DQ2	100	FBD<18> 18
	DQ3	1	FBD<19> 19
	DQ4	3	FBD<20> 20
	DQ5	4	FBD<21> 21
	DQ6	6	FBD<22> 22
	DQ7	7	FBD<23> 23
	DQ8	60	FBD<8> 8
	DQ9	61	FBD<9> 9
	DQ10	63	FBD<10> 10
	DQ11	64	FBD<11> 11
	DQ12	68	FBD<12> 12
	DQ13	69	FBD<13> 13
	DQ14	71	FBD<14> 14
	DQ15	72	FBD<15> 15
	DQ16	9	FBD<24> 24
	DQ17	10	FBD<25> 25
	DQ18	12	FBD<26> 26
	DQ19	13	FBD<27> 27
	DQ20	17	FBD<28> 28
	DQ21	18	FBD<29> 29
	DQ22	20	FBD<30> 30
	DQ23	21	FBD<31> 31
	DQ24	74	FBD<0> 0
	DQ25	75	FBD<1> 1
	DQ26	77	FBD<2> 2
	DQ27	78	FBD<3> 3
	DQ28	80	FBD<4> 4
	DQ29	81	FBD<5> 5
	DQ30	83	FBD<6> 6
	DQ31	84	FBD<7> 7

11 10 38 11 10 13 TERM_FBA<13>

11 10 33 22 FB2_5
NOSTUFF R383 270 5% 1/16W MF 603
R389 15 5% 1/16W MF 603
10 38 10 TERM_FBDQS1
NOSTUFF R382 270 5% 1/16W MF 603

FB2_5
R436 1K 1% 1/16W MF 603
R80 1K 1% 1/16W MF 603
C93 0.1uF N20P80% 16V CERM 603

11 10 33 22 FB2_5
NOSTUFF R40 270 5% 1/16W MF 603

R388 15 5% 1/16W MF 603
NOSTUFF R387 270 5% 1/16W MF 603

FB2_5
R81 1K 1% 1/16W MF 603
R86 1K 1% 1/16W MF 603
C81 0.1uF N20P80% 16V CERM 603

U21
SGRAM_2MX32
64MBIT
FLA
PROJECT
OMIT

FB2_5	VDD1	15	
	VDD2	35	
	VDD3	65	
	VDD4	96	
	VDDQ1	2	FB2_5
	VDDQ2	8	
	VDDQ3	14	
	VDDQ4	22	
	VDDQ5	59	
	VDDQ6	67	
	VDDQ7	73	
	VDDQ8	79	
	VDDQ9	86	
	VDDQ10	95	
11 10 38 TERM_FBA<0>	A0	31	
TERM_FBA<1>	A1	32	
TERM_FBA<2>	A2	33	
TERM_FBA<3>	A3	34	
TERM_FBA<4>	A4	47	
TERM_FBA<5>	A5	48	
TERM_FBA<6>	A6	49	
TERM_FBA<7>	A7	50	
TERM_FBA<8>	A8	51	
TERM_FBA<9>	A9	45	
TERM_FBA<10>	A10	36	
	CKE	53	
TERM_FBCLK0P	CK	55	
TERM_FBCLK0M	CK	54	
	CS	28	
	WE	25	
	CAS	26	
	RAS	27	
NO_TEST NC_SGRAM2RFU	RFU	93	
38 M_FBDQS5	DQS	94	
33 M_VREF2	VREF	58	
	DSF/MCL	52	
11 10 38 11 10 TERM_FBA<11>	BA0	29	
TERM_FBA<12>	BA1	30	
	VSSQ1	5	
	VSSQ2	11	
	VSSQ3	19	
	VSSQ4	62	
	VSSQ5	70	
	VSSQ6	76	
	VSSQ7	82	
	VSSQ8	92	
	VSSQ9	99	
	VSS1	16	
	VSS2	46	
	VSS3	66	
	VSS4	85	
	NC1	37	
	NC2	38	
	NC3	39	
	NC4	40	
	NC5	41	
	NC6	42	
	NC7	43	
	NC8	44	
	NC13	91	
	NC12	90	
	NC11	89	
	NC10	88	
	NC9	87	
	DM0	23	FBDQM<4> 4
	DM1	56	FBDQM<5> 5
	DM2	24	FBDQM<6> 6
	DM3	57	FBDQM<7> 7
	DQ0	97	FBD<32> 32
	DQ1	98	FBD<33> 33
	DQ2	100	FBD<34> 34
	DQ3	1	FBD<35> 35
	DQ4	3	FBD<36> 36
	DQ5	4	FBD<37> 37
	DQ6	6	FBD<38> 38
	DQ7	7	FBD<39> 39
	DQ8	60	FBD<40> 40
	DQ9	61	FBD<41> 41
	DQ10	63	FBD<42> 42
	DQ11	64	FBD<43> 43
	DQ12	68	FBD<44> 44
	DQ13	69	FBD<45> 45
	DQ14	71	FBD<46> 46
	DQ15	72	FBD<47> 47
	DQ16	9	FBD<48> 48
	DQ17	10	FBD<49> 49
	DQ18	12	FBD<50> 50
	DQ19	13	FBD<51> 51
	DQ20	17	FBD<52> 52
	DQ21	18	FBD<53> 53
	DQ22	20	FBD<54> 54
	DQ23	21	FBD<55> 55
	DQ24	74	FBD<56> 56
	DQ25	75	FBD<57> 57
	DQ26	77	FBD<58> 58
	DQ27	78	FBD<59> 59
	DQ28	80	FBD<60> 60
	DQ29	81	FBD<61> 61
	DQ30	83	FBD<62> 62
	DQ31	84	FBD<63> 63

11 10 38 11 10 13 TERM_FBA<13>

10 38 10 TERM_FBCKE
11 10 37 11 10 37 TERM_FBCLK0P
11 10 37 11 10 37 TERM_FBCLK0M
10 38 10 TERM_FBCS0*
10 38 TERM_FBWE*
10 38 TERM_FBCAS*
10 38 TERM_FBRAS*
10 38 10 TERM_FBDQS5

NOSTUFF R458 270 5% 1/16W MF 603
NOSTUFF R457 270 5% 1/16W MF 603

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6101	12

SCALE	SHT	OF
NONE	11	44

CR-12

GRAPHICS CHIP - UPPER 64-BIT DATA BUS & SUPPORT AND CENTER GROUND BALLS

NO_TEST			
			TRUE
NC_FBD<64>		AJ30	FBD64
NC_FBD<65>		AH29	FBD65
NC_FBD<66>		AG28	FBD66
NC_FBD<67>		AH30	FBD67
NC_FBD<68>		AF28	FBD68
NC_FBD<69>		AG30	FBD69
NC_FBD<70>		AG29	FBD70
NC_FBD<71>		AF30	FBD71
NC_FBD<72>		W28	FBD72
NC_FBD<73>		W29	FBD73
NC_FBD<74>		V27	FBD74
NC_FBD<75>		W30	FBD75
NC_FBD<76>		V28	FBD76
NC_FBD<77>		U27	FBD77
NC_FBD<78>		V30	FBD78
NC_FBD<79>		V29	FBD79
NC_FBD<80>		K28	FBD80
NC_FBD<81>		K27	FBD81
NC_FBD<82>		K30	FBD82
NC_FBD<83>		K29	FBD83
NC_FBD<84>		J27	FBD84
NC_FBD<85>		J30	FBD85
NC_FBD<86>		J29	FBD86
NC_FBD<87>		J28	FBD87
NC_FBD<88>		B27	FBD88
NC_FBD<89>		A27	FBD89
NC_FBD<90>		A26	FBD90
NC_FBD<91>		C26	FBD91
NC_FBD<92>		C25	FBD92
NC_FBD<93>		D24	FBD93
NC_FBD<94>		A25	FBD94
NC_FBD<95>		B25	FBD95
NC_FBD<96>		C21	FBD96
NC_FBD<97>		D21	FBD97
NC_FBD<98>		A21	FBD98
NC_FBD<99>		B21	FBD99
NC_FBD<100>		C20	FBD100
NC_FBD<101>		D20	FBD101
NC_FBD<102>		A19	FBD102
NC_FBD<103>		A20	FBD103
NC_FBD<104>		B15	FBD104
NC_FBD<105>		D16	FBD105
NC_FBD<106>		A15	FBD106
NC_FBD<107>		C15	FBD107
NC_FBD<108>		D15	FBD108
NC_FBD<109>		A14	FBD109
NC_FBD<110>		C14	FBD110
NC_FBD<111>		D14	FBD111
NC_FBD<112>		A7	FBD112
NC_FBD<113>		C7	FBD113
NC_FBD<114>		C5	FBD114
NC_FBD<115>		B6	FBD115
NC_FBD<116>		A5	FBD116
NC_FBD<117>		C6	FBD117
NC_FBD<118>		A6	FBD118
NC_FBD<119>		D7	FBD119
NC_FBD<120>		J3	FBD120
NC_FBD<121>		K4	FBD121
NC_FBD<122>		J2	FBD122
NC_FBD<123>		H1	FBD123
NC_FBD<124>		L4	FBD124
NC_FBD<125>		K3	FBD125
NC_FBD<126>		J1	FBD126
NC_FBD<127>		K2	FBD127

NO_TEST			
FBDQM8	AD29	NC_FBDQM<8>	TRUE
FBDQM9	AB29	NC_FBDQM<9>	TRUE
FBDQM10	G27	NC_FBDQM<10>	TRUE
FBDQM11	B30	NC_FBDQM<11>	TRUE
FBDQM12	C19	NC_FBDQM<12>	TRUE
FBDQM13	D19	NC_FBDQM<13>	TRUE
FBDQM14	D8	NC_FBDQM<14>	TRUE
FBDQM15	J4	NC_FBDQM<15>	TRUE
FBBCLK1	A10	NC_FBBCLK1	TRUE
FBBCLK0	B13	NC_FBBCLK0	TRUE

TP REQUIRED

U22
MONICA
(3 OF 3)
BGA

M12 M13 M14 M15 M16 M17 M18 M19 N12 N13 N14 N15 N16 N17 N18 N19 P12 P13 P14 P15 P16 P17 P18 P19 R12 R13 R14 R15 R16 R17 R18 R19 T12 T13 T14 T15 T16 T17 T18 T19 U12 U13 U14 U15 U16 U17 U18 U19 V12 V13 V14 V15 V16 V17 V18 V19 W12 W13 W14 W15 W16 W17 W18 W19

CENTER GND

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
359S0055	1	IC,SM530,SPREAD SPECTR CLK GEN,20P TSSOP	U19	PROJECT	G_SS

U19
IMISM530
TSSOP
OMIT

OSCIN 1
OSCOUT 2
AVDD 3
DVDD 12
OVDD 19
REFOUT 20
FOUT 15
LF 7
AVSS 8
DVSS 13
OVSS 18
R1 16
R0 17
S3 11
S2 14
S1 9
S0 6
SSON 10
D_C 4
STOP 5

G_SS
C69 22PF 5% CERM 603 50V
38 G_SSCLK_XI
PROJECT
G_SS
Y7 14.31818M SM
C88 22PF 5% CERM 603 50V
38 G_SSCLK_XO
G_SS

+3.3V
G_SSCLK_S3
G_SSCLK_S2
G_SSCLK_SSON
G_SSCLK_DC

R52 10K 1% 1/16W MF 603 G_SS NOSTUFF
R422 10K 1% 1/16W MF 603 G_SS
R55 10K 1% 1/16W MF 603 G_SS
R421 10K 1% 1/16W MF 603 NOSTUFF
R446 10K 1% 1/16W MF 603 G_SS NOSTUFF
R453 10K 1% 1/16W MF 603 G_SS
R445 10K 1% 1/16W MF 603 G_SS NOSTUFF
R452 10K 1% 1/16W MF 603 G_SS
R397 1K 1% 1/16W MF 603 G_SS

MODULATION SETTING [S3:S2]
00 = 1.25%
01 = 2.50%
10 = 5.00%
11 = 10.0%

MODULATION ENABLE
0 = MODULATION ON
1 = MODULATION OFF

DOWN/CENTER SPREAD
0 = DOWN SPREAD
1 = CENTER SPREAD

SELECTED OPTION IS THIS COLOR!

33 G_SSCLK_VDD

R50 10 1/10W 1% MF 603 G_SS +3.3V

C60 10UF N20P80% 16V CERM 1206 G_SS
C61 10UF N20P80% 16V CERM 1206 G_SS

Place a 10uF cap on each side of the SM530.

C55 0.1UF N20P80% 16V CERM 603 G_SS
C347 0.1UF N20P80% 16V CERM 603 G_SS
C41 0.1UF N20P80% 16V CERM 603 G_SS

Place one 0,1uF cap near each of the power pins.

R402 22 5% 1/16W G_SS MF 603
38 G_SSCLK_REFOUT
T_SSCLK_REFOUT 38 9

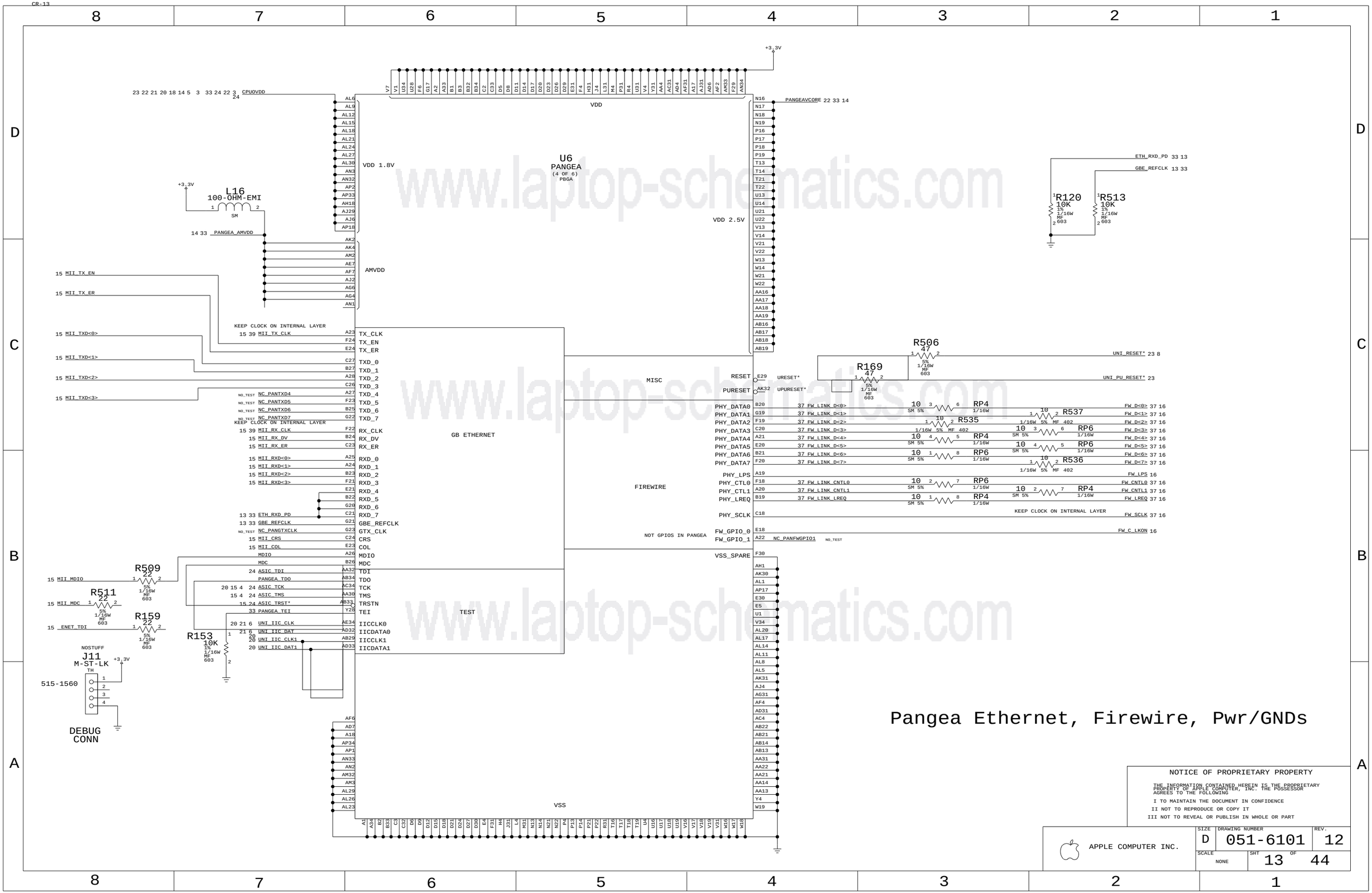
R406 22 5% 1/16W G_SS MF 603
38 G_SSCLK_MODOUT
GRAPH_XTALSIN 38 9

R913 and R914 must go near pins 20 and 15 of the SM530.

G_SSCLK_LF
R430 1K 1% 1/16W MF 603 G_SS
G_SSCLK_LFRC
C361 0.01UF 5% 50V CERM 603 G_SS
C80 0.001UF 5% 50V CERM 603 G_SS

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6101	12
SCALE: NONE	SHT 12 OF 44	



APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6101	12
SCALE: NONE	SHT 13 OF 44	

PANGEA CORE BYPASS

13 33 22 PANGEAVCORE

C492 C478 C515 C485 C468 C506 C480 C517 C493 C486 C469 C505 C514 C499 C479 C472 C507 C481 C516 C500 C482 C473 C508 C483 0.1UF 20% 10V CERM 402

C528 C465 C463 C462 4.7UF N20P80% 10V CERM 805

C504 C474 2.2UF N20P80% 10V CERM 805

PLACE AS NEAR AS CORE CENTER AS POSSIBLE

Pangea Processor I/F Bypass -- two per power/ground pair

18 13 5 3 33 24 22 3 24 23 22 21 20 CPUOVDD

C581 C557 C558 C559 C560 C561 C562 C563 C564 C565 C585 C580 C556 C546 C547 C548 C549 C550 C551 C552 C553 C583 0.1UF 20% 10V CERM 402

C477 C509 C464 C520 0.01UF 20% 10V CERM 402

Pangea I/O Ring Bypass -- two per power/ground pair

+3.3V

C484 C453 C567 C487 C415 C409 C410 C411 C421 C498 C436 C532 C518 C502 C489 C470 C460 C451 C541 0.1UF 20% 10V CERM 402

C570 C584 C526 C578 0.01UF 20% 10V CERM 402

+3.3V

C426 C427 C428 C429 C430 C431 C432 C433 C422 C447 C523 C511 C496 C476 C467 C456 C494 C424 0.1UF 20% 10V CERM 402

C420 0.01UF 20% 10V CERM 402

C527 C538 C566 0.01UF 20% 10V CERM 402

C571 0.1UF 20% 10V CERM 402

+3.3V

C488 C416 C412 C425 C417 C569 C437 C533 C519 C503 C490 C471 C461 C452 C438 C439 C440 C441 0.01UF 20% 10V CERM 402

C442 0.01UF 20% 10V CERM 402

C573 C574 C575 C576 2.2UF N20P80% 10V CERM 805

PLACE AT EDGES OF PROC I/F PLANE

+3.3V

C443 C444 C445 C434 C446 C522 C510 C495 C475 C466 C455 C454 C501 C497 C542 C413 C568 C423 C414 0.01UF 20% 10V CERM 402

C491 0.01UF 20% 10V CERM 402

Pangea AMVDD Bypass (one pair per pin)

13 33 PANGEA_AMVDD

C535 C525 C537 C544 C545 C572 0.01UF 20% 10V CERM 402

C529 C521 C536 C543 C554 C539 0.1UF 20% 10V CERM 402

C579 0.1UF 20% 10V CERM 402

+3.3V

C513 C459 C419 C418 C457 C512 2.2UF N20P80% 10V CERM 805

PLACE ALONG OUTSIDE OF BALL GRID ALONG 3 NON-MAXBUS MAXBUS SIDES (2 PER)

Pangea Bypass

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6101 | REV. 12

SCALE NONE | SHT 14 OF 44

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0024	1	CONN,PH JCK,RJ45,NO RJ11,SHLD,NMP,REFLW	J1	CRITICAL	

UPSIDE DOWN ETHERNET CONNECTOR?

ETHERNET CONN, RJ11 KEEPOUT

PLACE C921 NEAR U4'S VCCIO PINS.

ETHERNET PHY

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6101	12
SCALE: NONE	SHT 15 OF 44	

Firewire PHY and Termination

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0018	1	FLAS-64W431-H63,2PORT FW PHY,FW802A	REV A U17	PROJECT	
337S0509	1	FLAS-64W431-H63,2PORT FW PHY,FW802	REV 9 U17	PROJECT	OMIT
371S0058	1	DIODE,FAST RECOVERY,200V,3A,SMD	D13		
353S0094	1	5V FIXED/ADJ VREG, SOI-8	U18	PROJECT	OMIT
353S0275	1	3.3V FIXED/ADJ VREG, SOI-8	U18	PROJECT	
514-0023	2	CONN,RCPT,R/A,1394,NOFLANGES,NMP,6P	J4,J6	CRITICAL	

STUFF IF PMU SUPPLY OK NOISE MARGIN FOR FW

27 23 33 23 _3.8V_TRICKLE — NOSTUFF D2 MBR0530 SM — 33 3.3V_TO_FW — NOSTUFF L46 FERR-250-OHM SM — 16 33 FW_PHY_3_3

27 26 33 28 26 +12VSD — OMIT D13 MURS320T3 SM — 33 FW_VP_2 — CRITICAL F1 0.75AMP SM — 33 FW_VP_1 — L1 FERRITE-4532 SM

PHY_NOT_LEAKS R11 390K 5% 1/16W MF 603

PHY_LEAKS R12 47 5% 1/16W MF 603

C286 0.1UF 10% 50V CERM 1210

30 28 27 23 33 28 27 22 +12V_MAIN — R73 56 5% 1W FF 2512 — U22_8

I314 OMIT PLUS5VTAP U18 LP2951 SOI: IN, SENSE, SHUT, GND, OUT, ERR, FDBK — FW_VREG_FB

C45 1UF 20% 16V CERM 1206

C35 22UF 20% 4V ELEC SM

C29 22UF 20% 4V ELEC SM

16 33 FW_PHY_3_3

18 FWPHYRST — R60 2K 1% 1/16W MF 603 — FW_PHY_RST — Q3 2N3904 SM — R59 4.75K 1% 1/16W MF 603

R372 10K 1% 1/16W MF 603

C295 27PF 5% 50V CERM 603 — 37 FW_XI

CRITICAL Y1 24.576M SM

C305 27PF 5% 50V CERM 603 — 37 FW_XO

FW_PHY_RST*

FW_PHY_ISO*

16 13 16 13 12 FW_LPS — FW_LPS

16 13 37 16 13 37 FW_LREQ — FW_LREQ

OMIT PROJECT U17 FW802 FLAS

AVDD0	30	DVDD0	7
AVDD1	31	DVDD1	17
AVDD2	43	DVDD2	26
AVDD3	50	DVDD3	27
AVDD4	51	DVDD4	62
CPS	24	TPBIAS0	37 FW_BIAS1
XI	59	TPBIAS1	42 FW_BIAS2
XO	60	TPBIAS2	48
PD	19	TPA0+	36 FW_TPA1P
SE	28	TPA0-	35 FW_TPA1N
SM	29	TPB0+	34 FW_TPB1P
RESET	61	TPB0-	33 FW_TPB1N
ISO	23	TPA1+	41 FW_TPA2P
LPS	16	TPA1-	40 FW_TPA2N
LREQ	1	TPB1+	39 FW_TPB2P
PLLVDD	57	TPB1-	38 FW_TPB2N
SYSCLK	63	TPA2+	47
CTL0	3	TPA2-	46
CTL1	4	TPB2+	45
D0	5	TPB2-	44
D1	6	R0	54 FW_R0
D2	8	R1	55 FW_R1
D3	9	PC2	22
D4	10	PC1	21
D5	11	PC0	20
D6	12	PLLVSS	58
D7	13	C/LKON	18 FW_C_LKON 13
CNA	15		
DGND0	2	AGND0	32
DGND1	14	AGND1	49
DGND2	25	AGND2	52
DGND3	56	AGND3	53
DGND4	64		

FW_CPS

[OUT]

13 37 FW_SCLK — R15 22 1/16W 5% MF 603 — 37 FW_PHY_SCLK

13 37 FW_CNTL0 — R377 22 1/16W 5% MF 603 — 37 FW_PHY_CNTL0

13 37 FW_CNTL1 — R37 22 1/16W 5% MF 603 — 37 FW_PHY_CNTL1

13 37 FW_D<0>	R378 22 1/16W 5% MF 603	37 FW_PHY_D<0>
13 37 FW_D<1>	R36 22 1/16W 5% MF 603	37 FW_PHY_D<1>
13 37 FW_D<2>	R14 22 1/16W 5% MF 603	37 FW_PHY_D<2>
13 37 FW_D<3>	R379 22 1/16W 5% MF 603	37 FW_PHY_D<3>
13 37 FW_D<4>	R381 22 1/16W 5% MF 603	37 FW_PHY_D<4>
13 37 FW_D<5>	R13 22 1/16W 5% MF 603	37 FW_PHY_D<5>
13 37 FW_D<6>	R380 22 1/16W 5% MF 603	37 FW_PHY_D<6>
13 37 FW_D<7>	R34 22 1/16W 5% MF 603	37 FW_PHY_D<7>

C321 0.1UF N20P80% 16V CERM 603

R33 2K 1% 1/16W MF 603

R35 1K 1% 1/16W MF 603 — NO_TEST — NC_FW_CNA

R339 2.49K 1% 1/16W MF 603

R32 4.75K 1% 1/16W MF 603

C9 10PF 5% 50V CERM 603

C8 10PF 5% 50V CERM 603

C7 10PF 5% 50V CERM 603

C6 10PF 5% 50V CERM 603

R326 56.2 1% 1/16W MF 603

R325 56.2 1% 1/16W MF 603

C290 220PF 5% 25V CERM 603

R331 4.99K 1% 1/16W MF 603

C21 0.47UF 20% 16V CERM 805

R320 56.2 1% 1/16W MF 603

R323 56.2 1% 1/16W MF 603

C281 220PF 5% 25V CERM 603

R329 4.99K 1% 1/16W MF 603

C280 0.47UF 20% 16V CERM 805

C15 10PF 5% 50V CERM 603

C14 10PF 5% 50V CERM 603

C13 10PF 5% 50V CERM 603

C12 10PF 5% 50V CERM 603

R328 56.2 1% 1/16W MF 603

R327 56.2 1% 1/16W MF 603

R322 56.2 1% 1/16W MF 603

R324 56.2 1% 1/16W MF 603

FW_TPB2 — FW_TPB1

CRITICAL FL1 SM

37 FW_TPO1P	TPO
37 FW_TPO1N	TPO#
37 FW_TPI1P	TPI
37 FW_TPI1N	TPI#
33 16 FW_VP	VP
33 16 FW_VGND	VGND

OMIT CRITICAL 511-0023 J4 TH-UF1161C — PORT 1

C246 0.01UF 5% 50V CERM 603

C239 0.01UF 5% 50V CERM 603

CRITICAL FL3 SM

37 FW_TPO2P	TPO
37 FW_TPO2N	TPO#
37 FW_TPI2P	TPI
37 FW_TPI2N	TPI#
33 16 FW_VP	VP
33 16 FW_VGND	VGND

OMIT CRITICAL 511-0023 J6 TH-UF1161C — PORT 2

NOSTUFF C253 0.001UF 20% 50V CERM 603

C252 0.01UF 5% 50V CERM 603

C247 0.01UF 5% 50V CERM 603

L2 FERRITE-4532 SM

Firewire PHY

33 16 FW_PHY_3_3

AVDD BYPASS: C296 10UF N20P80% 16V CERM 1206; C24 0.01UF; C25 0.01UF; C18 0.01UF; C23 0.01UF; C26 0.01UF; C19 0.01UF

DVDD BYPASS: C319 10UF N20P80% 16V CERM 1206; C325 10UF N20P80% 16V CERM 1206; C27 0.01UF; C22 0.01UF; C20 0.01UF; C28 0.01UF; C34 0.01UF; C320 0.01UF

APPLE COMPUTER INC.

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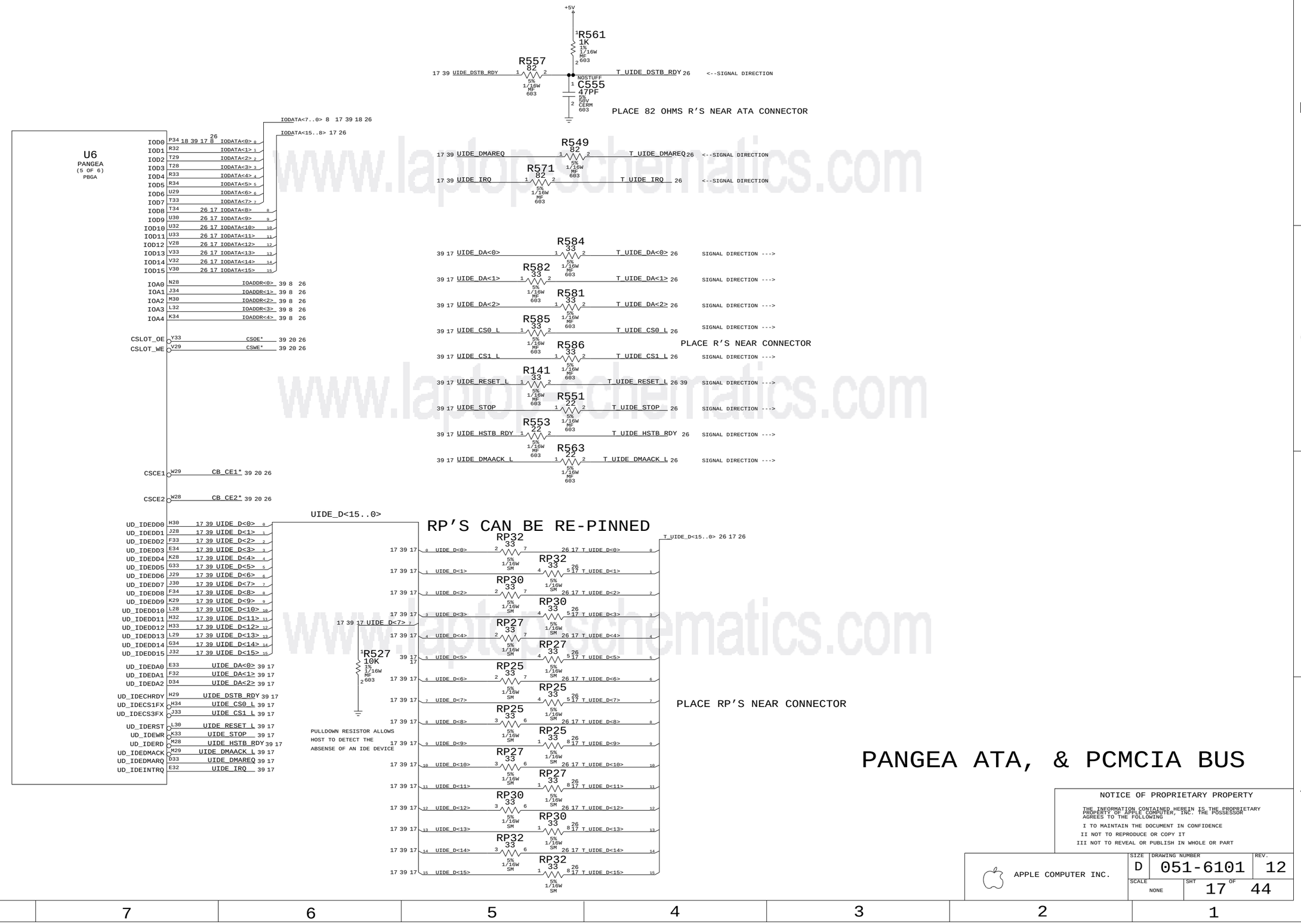

PANGEA ATA, & PCMCIA BUS

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6101	12
SCALE: NONE	SHT 17 OF 44	

+3.3V
R568 4.7 5% 1/16W MF 603
R544 4.7 5% 1/16W MF 603
R554 4.7 5% 1/16W MF 603
33 PANGEA_VDDA3
33 PANGEA_VDDA2
33 PANGEA_VDDA1
C582 1UF 10% 10V CERM 805
C534 1UF 10% 10V CERM 805
C540 1UF 10% 10V CERM 805
AP32 AJ30 AL33
VDDA_1 VDDA_2 VDDA_3
THIS COULD BE EMMO
IS SUPPOSED TO BE FW_PHY_SHUTDOWN
16 FWPHYRST
29 AUDIO_HW_RESET_L
R170 10K 1% 1/16W MF 603
WEAK PULLDOWN TO TERMINATE LINE UNTIL INITIALIZED
+3.3V
30 AUDIO_HP_MUTE
R168 10K 1% 1/16W MF 603
26 39 CB_RESET
20 15 ETHPHYRESETL
26 23 RING_DETECT*
20 23 PMU_INT
20 9 AGP_INTA*
32 AUDIO_SPKR_ID
R181 0 5% 1/16W MF 603
KW_EXTINT3
32 AUDIO_AMP_MUTE*
20 15 MDINT_L
KEEP R FOR ASIC PLL TESTING
20 23 PMU_NMI_IRQ*
26 20 39 CB_REG*
26 20 39 CB_IREQ*
30 AUDIO_HP_SENSE
18 CPU_INTR*
R512 0 5% 1/16W MF 603
23 PME*
+3.3V
R183 10K 1% 1/16W MF 603
KW_PME*
R175 0 5% 1/16W MF 603
23 KW_PROC_SLEEP_REQ*
518S0104
J27
U.FL-R_SMT
F-ST-SM
NOSTUFF
18 39 18 39 PAN_XI
FMAX_PAN_XI
R765 0 5% 1/16W MF 603
R764 49.9 1% 1/16W MF 603
NOSTUFF
R766 0 5% 1/16W MF 603
CRITICAL
Y6 18.4320M SM
Y6XI
39 PAN_XT
R569 0 5% 1/16W MF 603
C587 33PF 50V CERM 603
C588 33PF 50V CERM 603
R765.2 AND R766.1 TO SHARE PADS
CRYSTAL bias circuitry
needs to be looked at
to determine proper values
+3.3V
NOSTUFF
R173 10K 1% 1/16W MF 603
R172 0 5% 1/16W MF 603
23 STOPXTAL*
AVS_NO_1
23 KW_PEND_PROC_INT
PAN_XI
39 PAN_XO
PANGEA_STOPXTAL*
23 KW_WATCHDOG*
AK30 GPIO0
AA33 GPIO1
Y29 GPIO2
AF34 GPIO3
AB28 GPIO9
AE33 GPIO15
AC29 GPIO16
AC28 EXTINT0
AD30 EXTINT1
AG34 EXTINT2
AF33 EXTINT3
AF32 EXTINT4
AH34 EXTINT5
F27 EXTINT9
B31 EXTINT10
A32 EXTINT11
G27 EXTINT12
AF28 CPUINT0
G24 PCIPME
AK33 PROCSLEEPREQ IN
AL34 PENDPROCINT OUT
AK29 XTAL_IN
AH27 XTAL_OUT
AG28 STOPXTAL
AG30 WATCHDOG
CLOCKS
INTERRUPTS
MPIC
U6
PANGEA
(6 OF 6)
PBGA
GENERAL PURPOSE I/O'S
USB
CARDSLOT
AUDIO/I2S
IIC
AK34 SCCTXDA SCC_TXDA* 26
AE28 SCCRTSA SCC_RTSA* 26
AH33 SCCDTRA SCC_DTRA* 26
AJ34 SCCRXDA SCC_RXDA 26 20
AF30 SCCGPIOA SCC_GPIOA* 26 20
AF29 SCCTRXCA SCC_TRXCA 26 20
AD29 SCCTXDB PMU_MISO OUT 23
AG33 SCCRTSB PMU_REQ* OUT 20 23
AG32 SCCRXDB PMU_MOSI IN 23
AD28 SCCGPIOB PMU_ACK* IN 23
AE29 SCCTRXCB PMU_SCK IN 23
B28 VDD_USB 33 VDD_USB
C30 VSS_USB
B30 USB_VD1_P USB_DAP 39 19
C29 USB_VD1_N USB_DAM 39 19
A31 USB_VD2_P USB_DBP 39 19
E27 USB_VD2_N USB_DBM 39 19
F25 USB_PRTPWR0 USB_PWR_ABCD
E26 USB_PWRFLT0 USB_PWR_FLT 19 33
G26 USB_VD3_P USB_DCP 39 19
B29 USB_VD3_N USB_DCM 39 19
A30 USB_VD4_P USB_DDP 26
G25 USB_VD4_N USB_DDM 26
A29 USB_PRTPWR1 USB_PWR_ABCD
F26 USB_PWRFLT1
USB_PWR_ABCD 18 19 19 18 19 18 19
L33 IOA5 IOADDR<5> 39 8 26
N29 IOA6 IOADDR<6> 39 8 26
M32 IOA7 IOADDR<7> 39 8 26
L34 IOA8 IOADDR<8> 39 8 26
P28 IOA9 IOADDR<9> 39 8 26
M33 IOA10 IOADDR<10> 39 8 26
P29 IOA11 IOADDR<11> 39 8 26
M34 IOA12 IOADDR<12> 39 8 26
P30 IOA13 IOADDR<13> 39 8 26
N33 IOA14 IOADDR<14> 39 8 26
R28 IOA15 IOADDR<15> 39 8 26
P32 IOA16 IOADDR<16> 39 8 26
N34 IOA17 IOADDR<17> 39 8 26
R29 IOA18 IOADDR<18> 39 8 26
P33 IOA19 IOADDR<19> 39 8 26
R30 IOA20 IOADDR<20> 39 8 26
W34 CARDSLOT_IOWR CB_IOWR* 39 20 26
W33 CARDSLOT_IORD CB_IORD* 39 20 26
Y34 IOWAIT CB_WAIT* 39 20 26
AD34 AUD_DTO KW_AUD_DTO
AC32 AUD_DTI KW_AUD_DTI 29
AA29 AUD_SYNC KW_AUD_SYNC
AC33 AUD_BITCLK KW_AUD_BITCLK
AA28 AUD_CLKOUT PANAUDCLKOUT_PRE
H28 IICCLK_2 KW_IIC_CLK 26 29 20
C34 IICDATA_2 KW_IIC_DAT 26 29 20
OPTION ADD PARALLEL R TO
RESOLVE RESONANT NOISE CONCERN
+3.3V
L59 100-OHM-EMI SM
C400 0.01UF 5% 603 50V
R496 4.75K 1% 1/16W MF 603
R171 10 1/16W 1% MF 603
R155 10 1/16W 1% MF 603
SCR_SYNC 29 31
SCR_DATAIN 29
KW_AUD_DTI 29
R167 10 1/16W 1% MF 603
SCR_SCLK 29 31
R163 10K 1% 1/16W MF 603
NOSTUFF
R161 10K 1% 1/16W MF 603
R542 10 1/16W 1% MF 603
PANAUDCLKOUT 29 31
ROUTE AUDIO SIGNALS ON INTERNAL LAYERS
VSSA_1 VSSA_2 VSSA_3
AN31 AJ27 AG29
23 22 21 20 14 13 5 3 33 24 22 3 24 CPUOVDD
+3.3V
R336 4.75K 1% 1/16W MF 603
C299 0.1UF N20P80% 16V CERM 603
U16 74LCX125 14 TSSOP
NET13
R343 33 5% 1/16W MF 603
CPU_INT* 24 3
R10 2K 1% 1/16W MF 603
18 CPU_INTR*
NOSTUFF
R344 0 5% 1/16W MF 603
Pangea BootStrap Pins
+3.3V
NOSTUFF
R138 4.75K 1% 1/16W MF 603
R143 4.75K 1% 1/16W MF 603
R150 4.75K 1% 1/16W MF 603
R145 4.75K 1% 1/16W MF 603
R156 4.75K 1% 1/16W MF 603
R139 4.75K 1% 1/16W MF 603
R165 4.75K 1% 1/16W MF 603
R193 4.75K 1% 1/16W MF 603
26 18 39 17 8 IODATA<7..0>
0 IODATA<0>
1 IODATA<1>
2 IODATA<2>
3 IODATA<3>
4 IODATA<4>
5 IODATA<5>
6 IODATA<6>
7 IODATA<7>
R137 33.2K 1% 1/16W MF 603
R142 33.2K 1% 1/16W MF 603
R149 33.2K 1% 1/16W MF 603
R140 33.2K 1% 1/16W MF 603
R151 33.2K 1% 1/16W MF 603
R144 33.2K 1% 1/16W MF 603
R162 33.2K 1% 1/16W MF 603
R194 33.2K 1% 1/16W MF 603
1 = 66M 1 = SS ON 1 = Desktop
0 = 100M 0 = SS OFF 0 = Portable
1 = PCI1 Debug
0 = No PCI1
1 = PCI2 Debug
0 = No PCI2
11 = 33M AGP 0=66M
10 = 50M AGP 1=33M
01 = 40M AGP
00 = 66M AGP
PCI2 BUS CLK SPEED

PANGEA SER/AUD/USB, BOOTSTRAPS

APPLE COMPUTER INC.

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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0022	3	CONN,RCPT,USB,UPRIGHT R/A,NMP	J2,J3,J5	PROJECT	

PLACE NEAR PANGEA

R493 22 5% 1/16W MF 603 — 39 18 USB_DCM
R508 22 5% 1/16W MF 603 — 39 18 USB_DCP
R507 22 5% 1/16W MF 603 — 39 18 USB_DAM
R492 22 5% 1/16W MF 603 — 39 18 USB_DAP
R495 22 5% 1/16W MF 603 — 39 18 USB_DBM
R505 22 5% 1/16W MF 603 — 39 18 USB_DBP

L31 30-OHM-EMI SM — 39 USB_DCM_F — 39 19 USB_DCM_EMI
L29 30-OHM-EMI SM — 39 USB_DCP_F — 39 19 USB_DCP_EMI
L28 30-OHM-EMI SM — 39 USB_DAM_F — 39 19 USB_DAM_EMI
L27 30-OHM-EMI SM — 39 USB_DAP_F — 39 19 USB_DAP_EMI
L26 30-OHM-EMI SM — 39 USB_DBM_F — 39 19 USB_DBM_EMI
L25 30-OHM-EMI SM — 39 USB_DBP_F — 39 19 USB_DBP_EMI

R491 15K 1% 1/16W MF 603
R485 15K 1% 1/16W MF 603
R490 15K 1% 1/16W MF 603
R503 15K 1% 1/16W MF 603
R504 15K 1% 1/16W MF 603
R487 15K 1% 1/16W MF 603

KEEP STUB LENGTH SHORT

C235 33PF 5% 50V CERM 603
C236 33PF 5% 50V CERM 603
C237 33PF 5% 50V CERM 603
C238 33PF 5% 50V CERM 603
C244 33PF 5% 50V CERM 603
C245 33PF 5% 50V CERM 603

25 19 33 CHASSIS2

PLACE NEAR CONNECTOR

USB_FUSE
F2 2AMP-6V SM-1
+5V

33 19 USB_PWR

C284 0.1UF N20P80% 16V CERM 603
C283 0.1UF N20P80% 16V CERM 603
C277 0.1UF N20P80% 16V CERM 603

FL6 200-OHM SM
1 33 19 12 USB1_PWR
2 33 19 11 USB1_GND
3 33 19 10 USB2_PWR
4 33 19 9 USB2_GND
5 33 19 8 USB3_PWR
6 33 19 7 USB3_GND

C4 150UF 20% 6.3V TANT SMD
C2 150UF 20% 6.3V TANT SMD
C1 150UF 20% 6.3V TANT SMD

C267 0.01UF 5% 50V CERM 603
C249 0.01UF 5% 50V CERM 603
C254 0.01UF 5% 50V CERM 603
C266 0.01UF 5% 50V CERM 603
C241 0.01UF 5% 50V CERM 603
C248 0.01UF 5% 50V CERM 603
C265 0.01UF 5% 50V CERM 603
C243 0.01UF 5% 50V CERM 603
C240 0.01UF 5% 50V CERM 603

USB_SWITCH
U38 TPS2023 SOI
IN_0 IN_1 EN GND OUT_0 OUT_1 OUT_2 OC
18 USB_PWR_ABCD
USB_PWR_FLT 33 18

R335 10K 1% 1/16W MF 603
C751 0.1UF N20P80% 16V CERM 603

25 19 33 CHASSIS2

USB PORT 3

OMIT PROJECT
J5 F-RT-89485 TH-1
33 19 USB1_PWR
39 19 USB_DCM_EMI
39 19 USB_DCP_EMI
33 19 USB1_GND
514-0022
CHASSIS2 33 19 25
C278 0.01UF 5% 50V CERM 603

USB PORT 1

OMIT PROJECT
J3 F-RT-89485 TH-1
33 19 USB2_PWR
19 USB_DAM_EMI
39 USB_DAP_EMI
33 19 USB2_GND
514-0022
CHASSIS2 33 19 25
C279 0.01UF 5% 50V CERM 603

USB PORT 2

OMIT PROJECT
J2 F-RT-89485 TH-1
33 19 USB3_PWR
39 19 USB_DBM_EMI
39 19 USB_DBP_EMI
33 19 USB3_GND
514-0022
CHASSIS2 33 19 25
C270 0.01UF 5% 50V CERM 603

USB CONN & PWR

APPLE COMPUTER INC.

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D	051-6101	12
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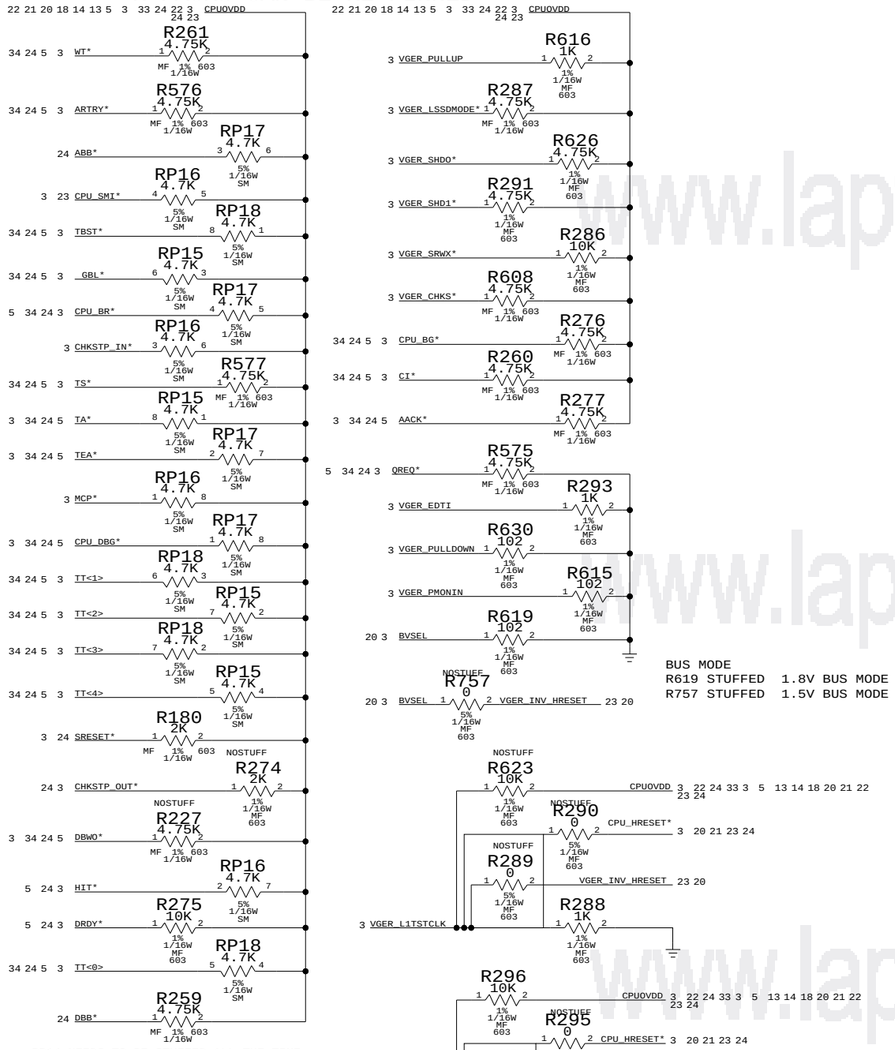
PROCESSOR PULLUP/PULLDOWN

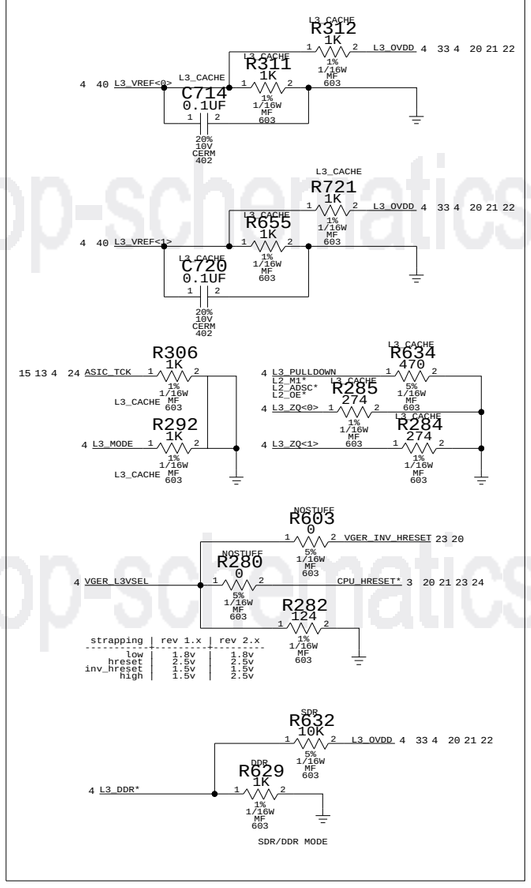
R-PACKS CAN BE RE-PINNED



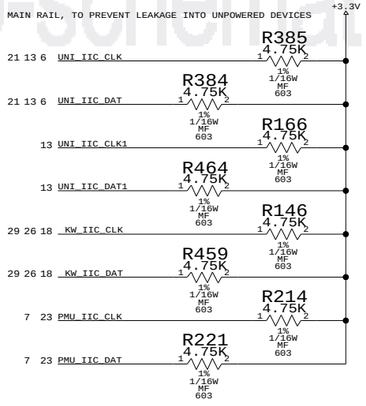
BUS MODE
R619 STUFFED 1.8V BUS MODE
R757 STUFFED 1.5V BUS MODE

BMODE <0>	BMODE <1>	MSSCR0 <16:17>	Sys Bus	Vger ID	Addr Drve
L	L	1 1	???	01	yes unavail
L	!hr	1 0	Max	01	yes unavail
L	hr	1 1	???	00	yes unavail
L	H	1 0	Max	00	yes unavail
hr	L	0 1	MB+	01	yes unavail
!hr	!hr	0 0	60x	01	yes unavail
!hr	hr	0 1	MB+	00	yes unavail
!hr	H	0 0	60x	00	yes unavail
hr	L	1 1	???	01	norm unavail
hr	!hr	1 0	Max	01	norm unavail
hr	hr	1 1	???	00	norm unavail
hr	H	1 0	Max	00	norm <----STUFF FOR THIS LINE
H	L	0 1	MB+	01	norm unavail
H	!hr	0 0	60x	01	norm
H	hr	0 1	MB+	00	norm unavail
H	H	0 0	60x	00	norm

L3 CACHE PULLUP/PULLDOWN

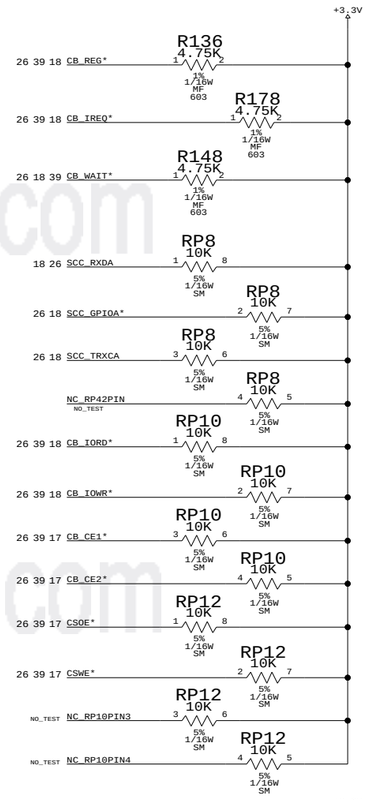


IIC BUS PULLUPS



PMU NOT RATED STRONG ENOUGH FOR 1K

PANGEA PULLUPS



MLB Pull-ups

APPLE COMPUTER INC.

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PULLUP FOR CPU_TMS IS ON SH 24, R519
PULLUP FOR CPU_TDI IS ON SH 24, R524
PULLUP FOR CPU_HRESET* IS ON SH 23, R202

PLACE NEAR R203

PLACE NEAR R203

L3_OVDD 1.8V

L3 CORE 2.5V

L3 VOLTAGE REGULATORS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
335S1005	1	IIC EEPROM 32KX8 SOIC	U36	IIC_256K_BLANK
341S1134	1	GROMIT SERIAL EEPROM PROGRAMMED	U36	IIC_PROGRAMMED

BOOTBANGER

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6101	12
SCALE: NONE	SHT 21 OF 44	

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VGER_VCORE	R258	R262
1.3V	36.5K	7.5K
1.35V	36.5K	8.45K
1.4V	7.5K	NOSTUFF
1.45V	8.2K	NOSTUFF
1.5V	36.5K	11.5K
1.55V	36.5K	12.7K
1.6V	10K	NOSTUFF
1.65V	36.5K	15.0K
1.7V	36.5K	16.2K
1.75V	11.8K	NOSTUFF
1.8V	36.5K	19.0K
1.85V	36.5K	20.4K
1.9V	36.5K	22.0K
1.95V	36.5K	23.7K
2.0V	15K	NOSTUFF
2.05V	36.5K	27.3K
2.10V	36.5K	29.2K
2.15V	16.9K	NOSTUFF

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
131S6812	1	CAP,CER,68PF,5%,50V,603	C184		

VGER_VCORE SET FOR 1.65V

GRAPHICS CORE IS SET TO 1.90V

SET FOR 1.8V CPUOVDD

SET FOR 2.5V VIDEO FRAME BUFFER

SET FOR 2.5V PANGEA CORE

MUST STRADDLE CPUOVDD/3.3V PLANE BREAK

DON'T EVER STUFF THIS CONN NOT FIT ON PCB FOR DANNY ITANI FMAX!!!

515-1563

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6101	12
SCALE: NONE	SHT 22 OF 44	

Voltage Regulators

CR-23

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S0543	1	PROGRAMMED PMU,M16C62	U8	PROJECT	OMIT
337S0267	1	BLANK, PMU,M16C62, 64KB	U8	PROJECT	OMIT
337S0270	1	BLANK, PMU,M16C62, 256KB	U8	PROJECT	OMIT
341S0618	1	PMU,M16C62,64KB,V66B	U8	PROJECT	
110S2003	1	2K RESISTOR	R202		VGER_GOOD
110S1003	1	1K RESISTOR	R202		VGER_FIX

Power Manager Unit

APPLE COMPUTER INC.

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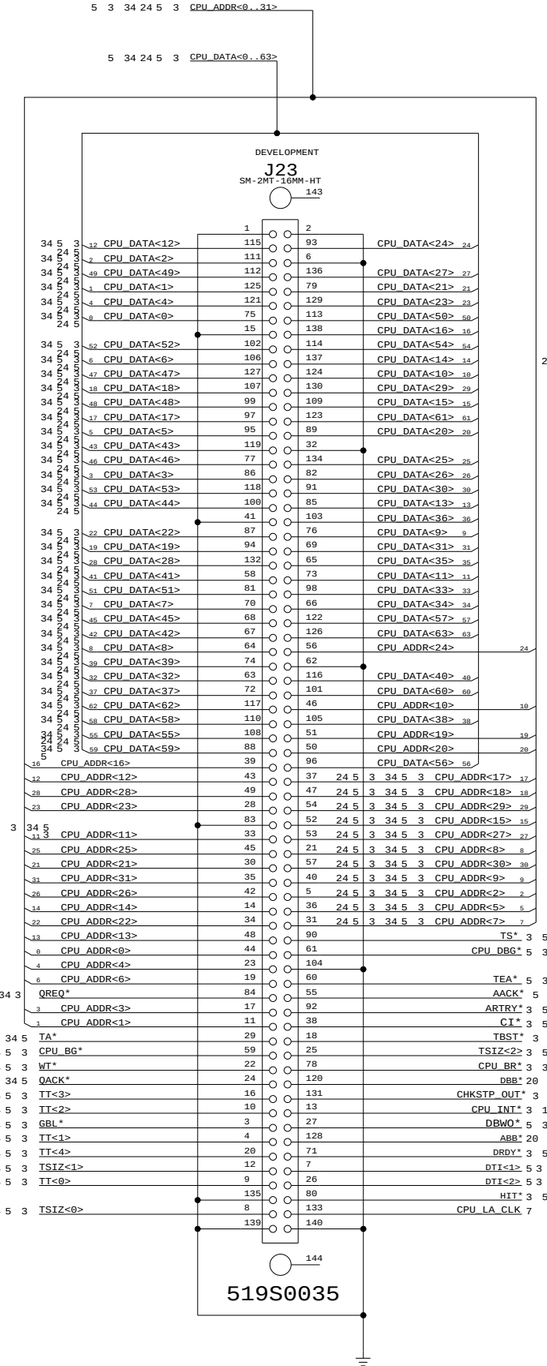
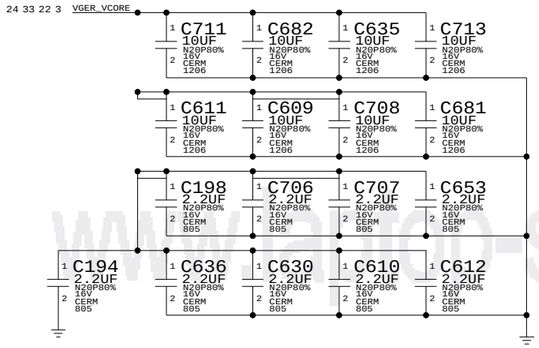
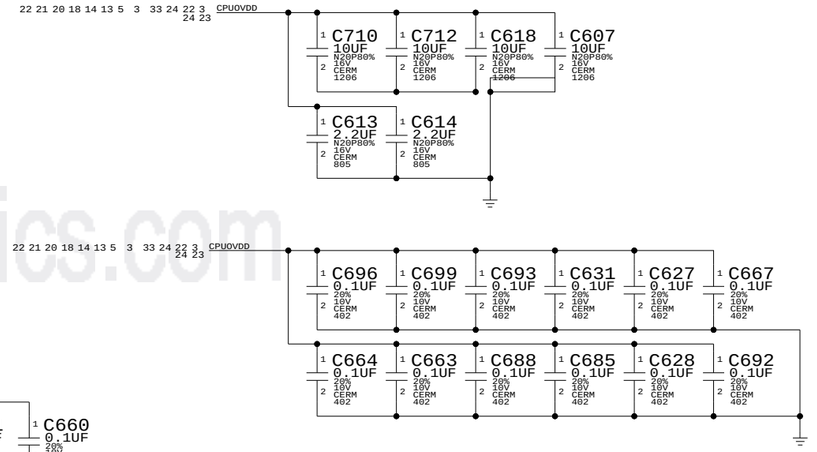
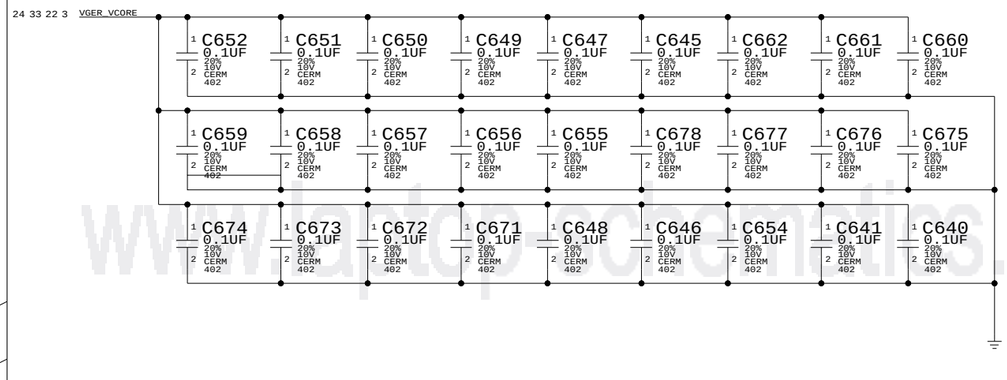
D	051-6101	12
SCALE: NONE	SHT 23 OF 44	

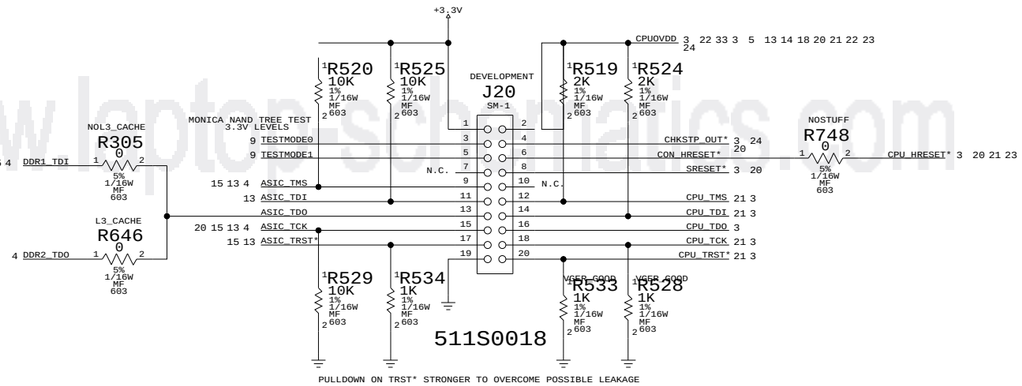


CPU BUS LOGIC ANALYZER CONNECTOR









PULLDOWN ON TRST* STRONGER TO OVERCOME POSSIBLE LEAKAGE

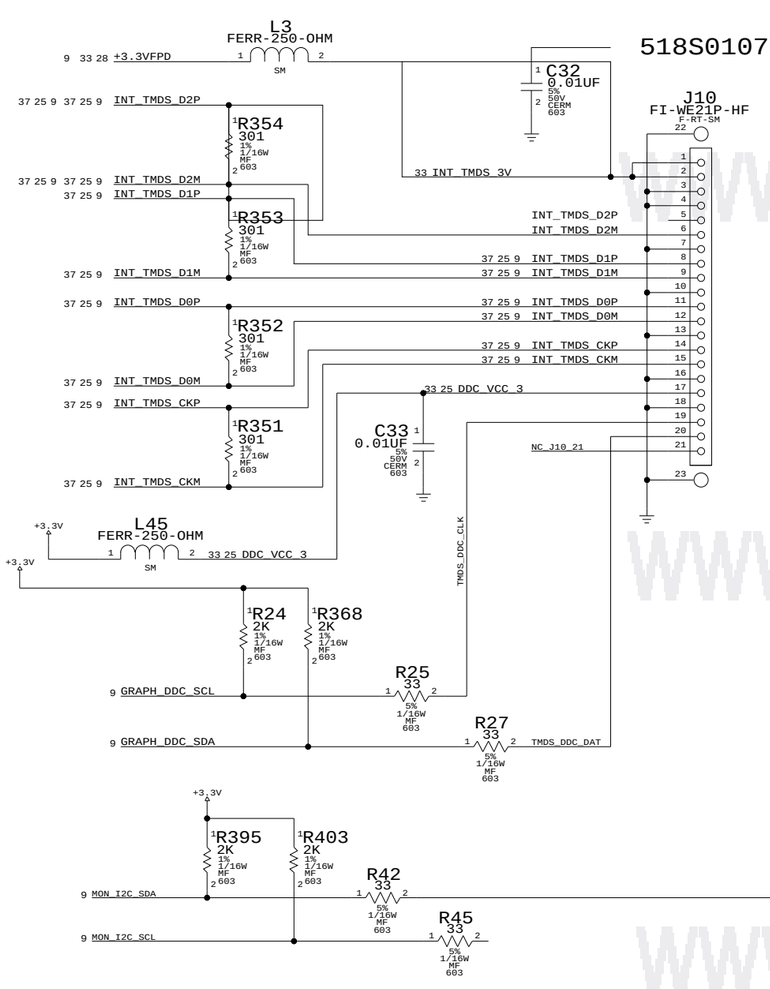
ESP, LA Connectors

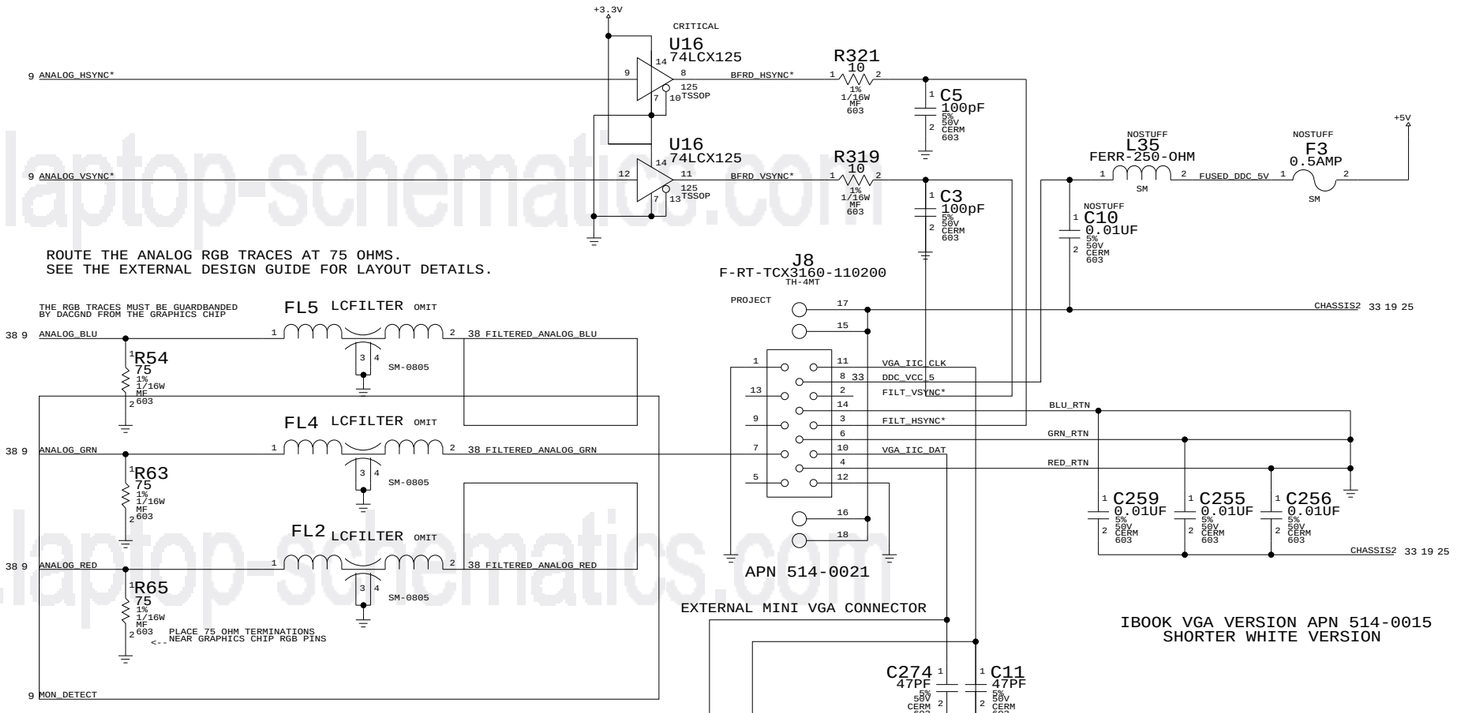
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6101	12
SCALE: NONE	SHT 24 OF 44	

INTERNAL TMDS CONNECTOR, EXTERNAL VGA CONNECTOR AND GRAPHICS CHIP STRAP OPTIONS

Internal TMDS Connector

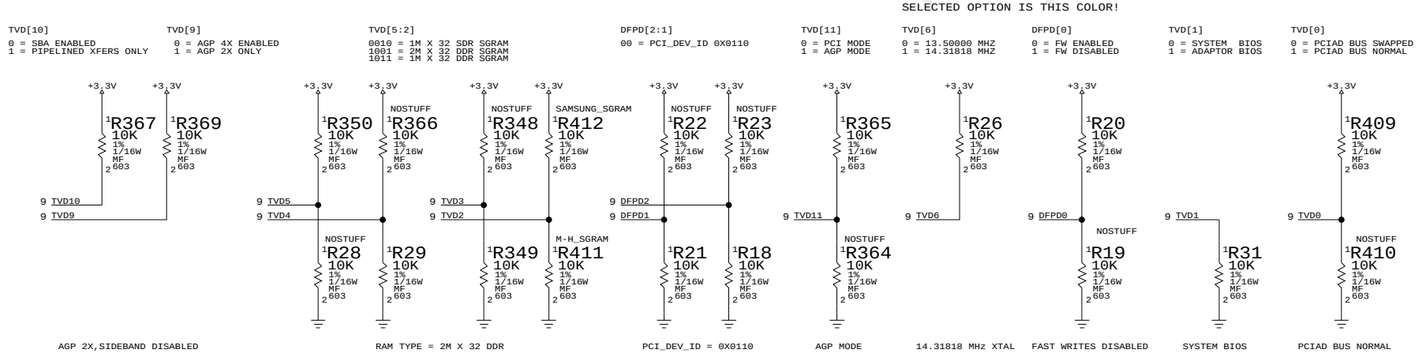




PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
155S0012	3	FILTER_LC	FL5,FL4,FL2		

APN 155S0012 DOESN'T EXIST IN DATABASE, SYMBOLS ARE 155S0010

SELECTED OPTION IS THIS COLOR!



APPLE COMPUTER INC.

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SCALE: NONE	SHT 25 OF 44	

CR-26

CD/HD SLOT

17 26 17 T_UIDE_D<15..0>

+5V

R526 10K 1% 1/16W MF 603 — 17 39 T_UIDE_RESET_L

R567 10K 1% 1/16W MF 603

J14 ST-NC20 TH

7	T_UIDE_D<7>	4	26 17 T_UIDE_D<8> 8
6	T_UIDE_D<6>	6	26 17 T_UIDE_D<9> 9
5	T_UIDE_D<5>	8	26 17 T_UIDE_D<10> 10
4	T_UIDE_D<4>	10	26 17 T_UIDE_D<11> 11
3	T_UIDE_D<3>	12	26 17 T_UIDE_D<12> 12
2	T_UIDE_D<2>	14	26 17 T_UIDE_D<13> 13
1	T_UIDE_D<1>	16	26 17 T_UIDE_D<14> 14
0	T_UIDE_D<0>	18	26 17 T_UIDE_D<15> 15

NOSTUFF R573 1K 1% 1/16W MF 603

R555 10K 1% 1/16W MF 603

17 T_UIDE_DMAREQ

17 T_UIDE_STOP

17 T_UIDE_HSTB_RDY

17 T_UIDE_DSTB_RDY

UTADETECT_L

UIDE_CSEL

17 T_UIDE_DMAACK_L

17 T_UIDE_IRQ

33 UIDE_IOCS16_L

17 T_UIDE_DA<1>

17 T_UIDE_DA<0>

NET29

T_UIDE_DA<2> 17

17 T_UIDE_CS0_L

J15 39

17 T_UIDE_CS1_L

DEVELOPMENT DS2 GREEN SM — NET42

DEVELOPMENT R593 330 5% 1/16W MF 603

R545 4.75K 1% 1/16W MF 603

C591 100pF 5% 50V CERM 603

R574 4.75K 1% 1/16W MF 603

C596 100pF 5% 50V CERM 603

CRITICAL

515-1588

NOSTUFF C590 0.047uF 5% 50V CERM 603

C595 100pF 5% 50V CERM 603

R559 0 5% 1/16W MF 603

UATADETECT IS NOT USED BY PANGEA ANYMORE
PULLUP COULD BE DELETED LATER
SAVE FOR NOW

HD/CD SIGNALS SHARE THIS CABLE (ATA5 & ATA4)
HD/CD POWER COMES FROM DC/DC CONNECTOR J18 SH26

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
516S1007	1	CONN,HDR,R/A,PCMCIA,LG SLD PDS,68P BLK	J22	PROJECT	
516S0008	1	CONN,SMT,PCMCIA,SHORT ARMS	J22	PROJECT	OMIT
516S0013	1	CONN,HDR,R/A,PC CARD,LRGE SOLD PADS,68P	J22	PROJECT	OMIT
860-1034	2	MODEM_STANDOFF STDOFF-19709-236H-TH	ZH40,ZH44	PROJECT	

STUFF IF CARDBUS HAS 5V SIGNAL LEVELS

CARDSLOT POWER CONTROL NOT SUPPORTED

+3.3V

C139 10UF N20P80% 16V CERM 1206

C140 10UF N20P80% 16V CERM 1206

C143 0.01UF 5% 50V CERM 603

C144 0.1UF N20P80% 16V CERM 603

PCMCIA (WIRELESS) SLOT
APN 516S0013 (FOXCONN SHORT ARMS, SOLDER PADS)

J22 SMC-4MT

NO_TEST	NC_PCMCIACH1	69		
	OMIT	35	1	
NO_TEST	NC_CB_DETECT1*	36	2	ROMD3/PCIAD3 IOADATA<3> 8 17 39 18
17 IODATA<11>	PCIAD11	37	3	ROMD4/PCICBE0 IOADATA<4> 8 17 39 18
17 IODATA<12>	PCIAD12	38	4	ROMD5/PCICBE1 IOADATA<5> 8 17 39 18
17 IODATA<13>	PCIAD13	39	5	ROMD6/PCICBE2 IOADATA<6> 8 17 39 18
17 IODATA<14>	PCIAD14	40	6	ROMD7/PCICBE3 IOADATA<7> 8 17 39 18
17 IODATA<15>	PCIAD15	41	7	CB_CE1* 17 39 20
20 39 17 CB_CE2*		42	8	ROMA10/PCIAD26 IOADDR<10> 18 39 8
NO_TEST	NC_VSENSE1*	43	9	CS1 == OE CSOE* 17 39 20
20 39 18 CB_IORD*		44	10	ROMA11/PCIAD27 IOADDR<11> 18 39 8
20 39 18 CB_IOWR*		45	11	ROMA9/PCIAD25 IOADDR<9> 18 39 8
8 39 18 IOADDR<17>	ROMA17/PCISTOP	46	12	ROMA8/PCIAD24 IOADDR<8> 18 39 8
8 39 18 IOADDR<18>	ROMA18/PCITRDY	47	13	ROMA13/PCIAD29 IOADDR<13> 18 39 8
8 39 18 IOADDR<19>	ROMA19/PCIIRDY	48	14	ROMA14/PCIAD30 IOADDR<14> 18 39 8
8 39 18 IOADDR<20>	ROMA20/PCIFRAME	49	15	CS3 == WE CSWE* 17 39 20
7 LACLK	NIC TDI/PCIAD21	50	16	CB_IREQ* 18 39 20
		51	17	+3.3V
26 8 NIC TDO/PCIAD22	ROM_ONBOARD_CS*	52	18	
8 6 T_ROMWE*	NIC TCK/PCIAD23	53	19	ROMA16/PCIDEVSEL IOADDR<16> 18 39 8
NOT T_ROMOE* IN P7 6 ROMOE*	NIC ETSYN/PCIAD24	54	20	ROMA15/PCIAD31 IOADDR<15> 18 39 8
NIC ETCK/PCIAD25	T_ROMCS*	55	21	ROMA12/PCIAD28 IOADDR<12> 18 39 8
NO_TEST NC_VSENSE2*		56	22	ROMA7/PCIAD23 IOADDR<7> 18 39 8
39 18 CB_RESET		57	23	ROMA6/PCIAD22 IOADDR<6> 18 39 8
20 18 39 CB_WAIT*		58	24	ROMA5/PCIAD21 IOADDR<5> 18 39 8
NO_TEST NC_INP_ACK		59	25	ROMA4/PCIAD20 IOADDR<4> 18 39 8
20 39 18 CB_REG*		60	26	ROMA3/PCIAD19 IOADDR<3> 18 39 8
NIC_JTAG_RESET	NIC JTAG RESET-H/CB SPEAKER	61	27	ROMA2/PCIAD18 IOADDR<2> 18 39 8
NO_TEST NC_STAT_CHG		62	28	ROMA1/PCIAD17 IOADDR<1> 18 39 8
17 IODATA<8>	PCIAD8	63	29	ROMA0/PCIAD16 IOADDR<0> 18 39 8
17 IODATA<9>	PCIAD9	64	30	ROMD0/PCIAD0 IODATA<0> 8 17 39 18
17 IODATA<10>	PCIAD10	65	31	ROMD1/PCIAD1 IODATA<1> 8 17 39 18
33 DETECT_5VT		66	32	ROMD2/PCIAD2 IODATA<2> 8 17 39 18
		67	33	NC_CB_CS16* NO_TEST
NC_PCMCIACH2		68	34	KEEP CLOCKS ON INTERNAL LAYERS
NO_TEST		70		

+3.3V

R132 4.75K 1% 1/16W MF 603

NOSTUFF R133 0 5% 1/16W MF 603 — 23 IO_RESET*

NOSTUFF R131 499 1% 1/16W MF 603 — 33 DETECT_5VT

R157 1K 1% 1/16W MF 603 — 26 6 26 6 T_ROMCS* — ROM_ONBOARD_CS* 8 26

MODEM SLOT

+3.3V

C391 10UF N20P80% 16V CERM 1206

C385 0.1UF N20P80% 16V CERM 603

J12 SM-2MT-6MM-HT

20 18 MODEM_SDOWN	1	2	
NO_TEST NC_MODEM_DETECT_L	3	4	MODEM_RESET* 18 20
18 SCC_DTRA*	5	6	SCC_RTSA* 18
	7	8	
18 SCC_TXDA*	9	10	SCC_RXDA 18 20
20 18 SCC_TRXCA	11	12	SCC_GPIOA* 18 20
NO_TEST NC_DAA_CLKOUT	13	14	
NO_TEST NC_DAA_LOADOUT	15	16	RING_DETECT* 18 23
NO_TEST NC_-10VUNREG	17	18	NC_-12VREG NO_TEST
20 29 18 KW_IIC_CLK	19	20	+12VSD 26 28 33 16 26 27
20 29 18 KW_IIC_DAT	21	22	+12V NEEDS TO BE 25 MIL TRACE
	23	24	26 USB_DDP_T
	25	26	26 USB_DDM_T
	27	28	
	29	30	AUD_MODEM_RTN 31
	31	32	AUD_MODEM 31
	33	34	NC_AUDIO2MODEM NO_TEST
	35	36	NC_AUDIO2MODEMRTN NO_TEST
	37	38	
	39	40	
	43		

+3.3V R483 4.75K 1% 1/16W MF 603

+5V

PIN 35 IIC ADDRESS
WE ARE SET TO ADDR= AC

C384 10UF N20P80% 16V CERM 1210

C381 0.1UF N20P80% 16V CERM 603

515S0120

CRITICAL

OMIT ZH40 STDOFF-197OD-236H-TH — NC_ZH40 1

OMIT ZH44 STDOFF-197OD-236H-TH — NC_ZH44 1

R475 22 5% 1/16W MF 603 — 18 USB_DDP — 26 USB_DDP_T

R478 22 5% 1/16W MF 603 — 18 USB_DDM — 26 USB_DDM_T

R477 15K 1% 1/16W MF 603

R476 15K 1% 1/16W MF 603

PLACE NEAR PANGEA
KEEP STUB LENGTH SHORT

L58 FERR-250-OHM — 31 28 27 21 33 28 +5VSD — 26 KS5VSD

L66 FERR-250-OHM — 33 LED_5V — 26 LED_5V_FILT

R521 82.5 1% 1/4W FF 1210

L56 FERR-250-OHM — 9 INV_CUR_HI — 26 INV_CUR_HI_FILT

L62 FERR-250-OHM — 9 LCD_PWM — 26 LCD_PWM_FILT

L57 FERR-250-OHM — 27 16 33 28 26 +12VSD — 26 +12VSD_FILT

L44 1000-OHM-EMI — PWR_SWITCH* — 26 ON_SWITCH*

S3 SM — S34 / S32

L43 1000-OHM-EMI

SWI_4RTSA1_SMB_1

L64 1000-OHM-EMI

L65 1000-OHM-EMI — 26 SWITCH_GND

L63 1000-OHM-EMI — 28 33 LED_RET — 26 LED_RET_FILT

L60 FERR-250-OHM — 9 LAMP_STS — 26 LAMP_STS_FILT

+3.3V

L55 NOSTUFF FERR-250-OHM — 33 J14_10

L51 NOSTUFF FERR-250-OHM — 26 J14_6

FAN CONTROL

NOSTUFF J24 SM-2MT

NO_TEST	5	NC_J24.5
FAN_CTL	1	
	2	
NO_TEST	6	NC_J24.6

APN 515-1720

L67 NOSTUFF FERR-250-OHM — 26 FAN_CTL_FILT

C62 47UF 20% 16V ELEC SM

C387 0.01UF 5% 50V CERM 603

C398 0.01UF 5% 50V CERM 603

C138 47UF 20% 16V ELEC SM

C393 1UF 10% 10V CERM 805

C399 220PF 5% 25V CERM 603

C392 220PF 5% 25V CERM 603

C403 0.01UF 5% 50V CERM 603

C408 0.01UF 5% 50V CERM 603

C402 0.01UF 5% 50V CERM 603

C397 220PF 5% 25V CERM 603

NOSTUFF C382 220PF 5% 25V CERM 603

NOSTUFF C372 220PF 5% 25V CERM 603

NOSTUFF C717 220PF 5% 25V CERM 603

(KITCHEN SINK) CONNECTOR
INT MIC/SPEAKER

C368 100PF 5% 50V CERM 603

C363 100PF 5% 50V CERM 603

J13 SM

31 MIC1SHLD	1	2	
31 MIC1HIGH	3	4	KS_INT_SPKR+ 32
31 MIC1LOW	5	6	NEW_KS_INT_SPKR- 32
	7	8	26 J14_6
NO_TEST NC_MIC2A	9	10	NC_EXT_28V/12V NO_TEST
NO_TEST NC_MIC2B	11	12	J14_10
NO_TEST NC_MIC2C	13	14	NC_EXT_ENGAGED NO_TEST
26 INV_CUR_HI_FILT	15	16	26 FAN_CTL_FILT
33 26 KS5VSD	17	18	+12VSD_FILT INV 12V
26 LCD_PWM_FILT	19	20	
(DELTA_POWER) 26 ON_SWITCH*	21	22	26 LAMP_STS_FILT
PROX SWITCH POWER LED_5V_FILT	23	24	33 26 LED_RET_FILT
27 26 16 33 28 26 +12VSD FAN 12V	25	26	26 SWITCH_GND

515S0863

APPLE COMPUTER INC.

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KITCHEN SINK, PCMCIA, HD/CD, MODEM CONNECTORS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
518-0011	1	CONN,HDR,STR,3MM PTCH,14-P,REFLOW	J15	PROJECT	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0360	138S0321		C200,C644,C643,C199	

RFA 147354
518-0011

DC/DC CONVERTER
5V AND 3.3V
POWER CONNECTOR

PLACE CAPS AS CLOSE AS POSSIBLE TO FETS 28 27 23 16 33 28 27 22 +12V_MAIN 30

APPLE COMPUTER INC.

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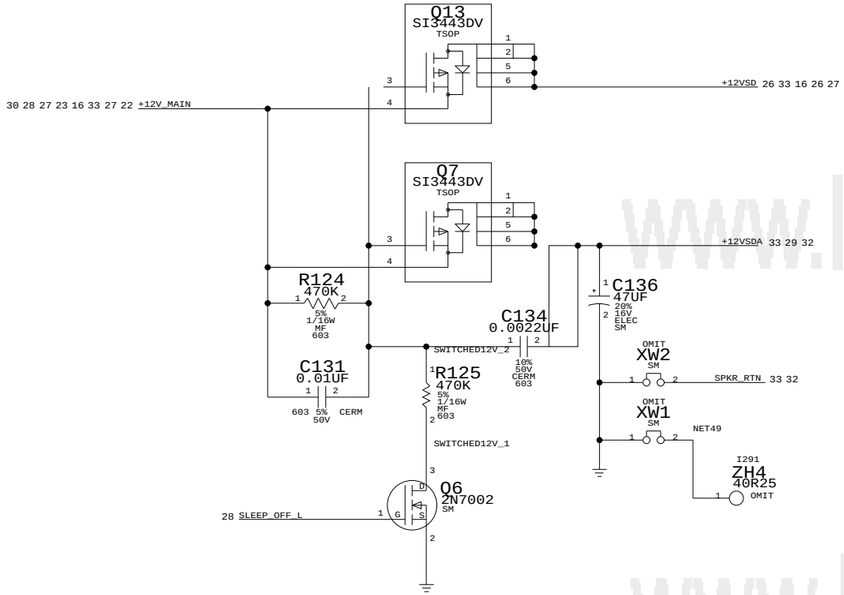
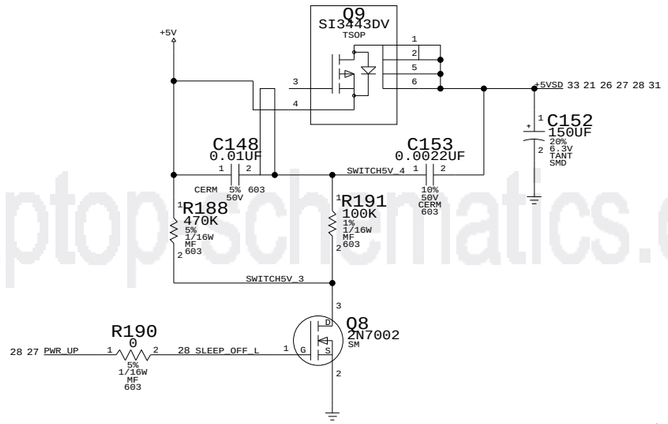
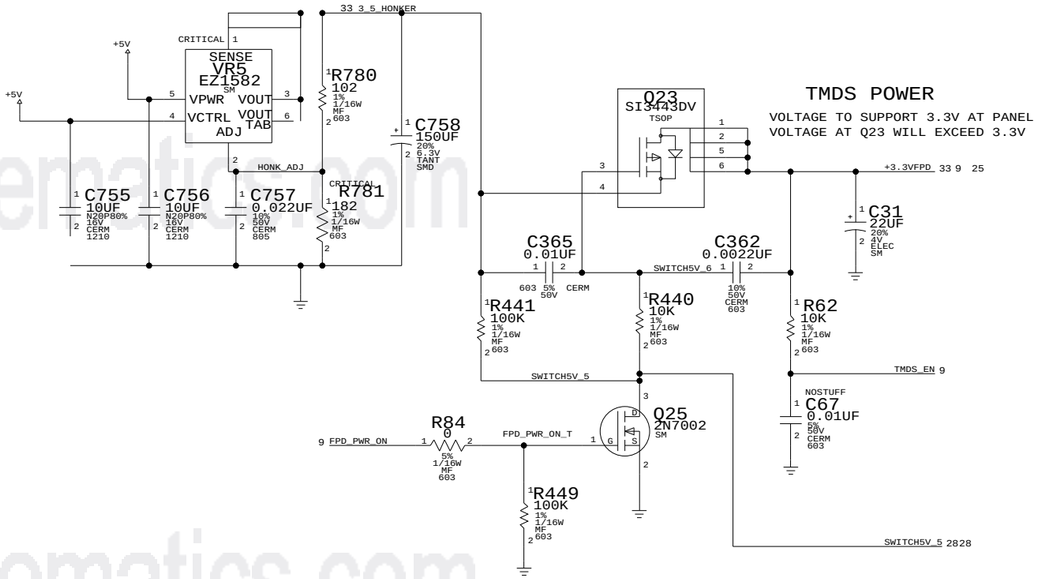
D	051-6101	12
SCALE: NONE	SHT 27 OF 44	

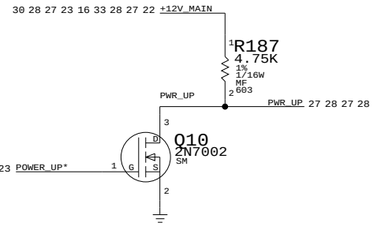




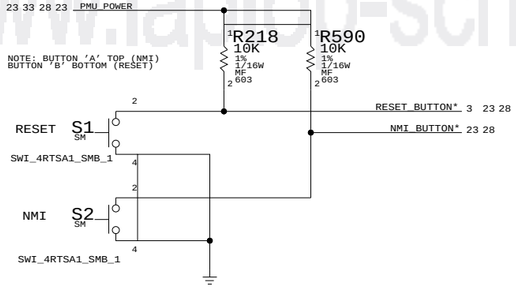


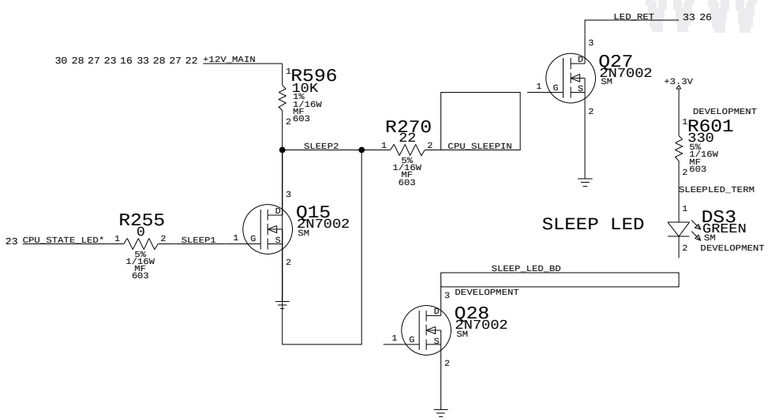
TMDS POWER

VOLTAGE TO SUPPORT 3.3V AT PANEL
VOLTAGE AT Q23 WILL EXCEED 3.3V

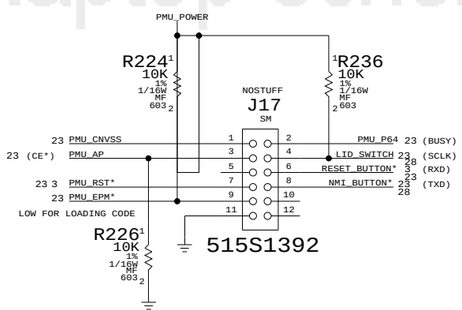


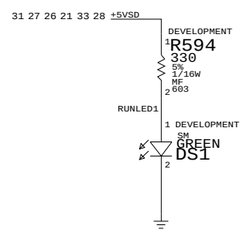
CPU SLEEP LED CKT FROM TRINITY





SERIAL DOWNLOAD CONNECTOR





PMU SERIAL DL, LPWR CTRL, TMDS POWER

APPLE COMPUTER INC.

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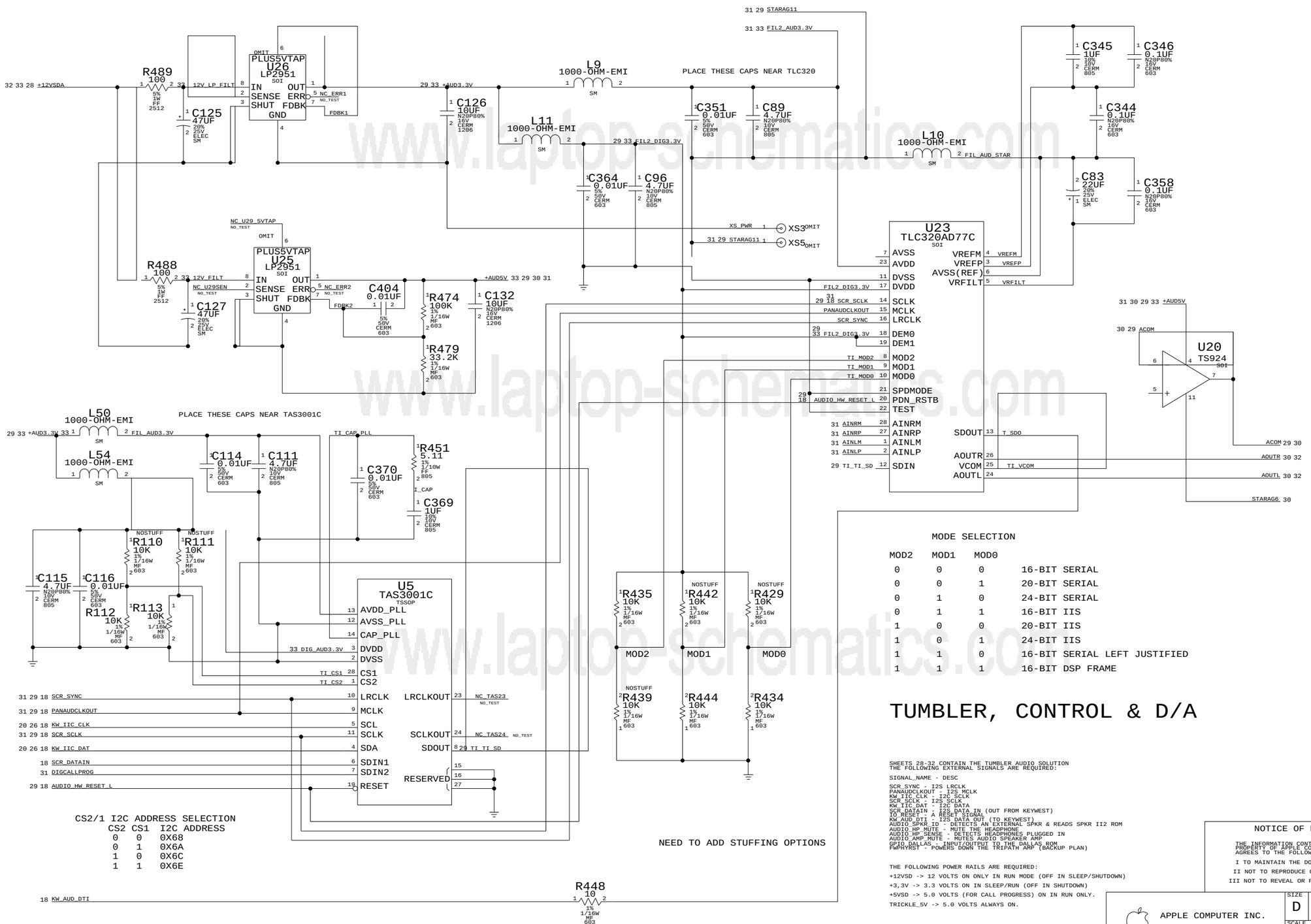
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S0275	2	IC,2951,ADJ,UPWR,REG,8P,SOP	U25,U26		



MODE SELECTION

MOD2	MOD1	MOD0	
0	0	0	16-BIT SERIAL
0	0	1	20-BIT SERIAL
0	1	0	24-BIT SERIAL
0	1	1	16-BIT IIS
1	0	0	20-BIT IIS
1	0	1	24-BIT IIS
1	1	0	16-BIT SERIAL LEFT JUSTIFIED
1	1	1	16-BIT DSP FRAME

CS2/1 I2C ADDRESS SELECTION

CS2	CS1	I2C ADDRESS
0	0	0X68
0	1	0X6A
1	0	0X6C
1	1	0X6E

NEED TO ADD STUFFING OPTIONS

TUMBLER, CONTROL & D/A

SHEETS 28-32 CONTAIN THE TUMBLER AUDIO SOLUTION
THE FOLLOWING EXTERNAL SIGNALS ARE REQUIRED:

SIGNAL_NAME - DESC

SCR_SYNC - I2S LRCLK
PANAUDCLKOUT - I2S MCLK
KW_IIC_CLK - I2C SCLK
SCR_SCLK - I2S SCLK
KW_IIC_DAT - I2C DATA
SCR_DATAIN - I2S DATA IN (OUT FROM KEYWEST)
KW_RESET_L - A RESET SIGNAL
KW_AUD_DTI - I2S DATA OUT (TO KEYWEST)
AUDIO_SPKR_ID - DETECTS AN EXTERNAL SPKR & READS SPKR II2 ROM
AUDIO_HP_MUTE - MUTE THE HEADPHONE
AUDIO_HP_SENSE - DETECTS HEADPHONES PLUGGED IN
AUDIO_AMP_MUTE - MUTES AUDIO SPEAKER AMP
GPIO_DALLAS - INPUT/OUTPUT TO THE DALLAS ROM
FWPHYRST - POWERS DOWN THE TRIPATH AMP (BACKUP PLAN)

THE FOLLOWING POWER RAILS ARE REQUIRED:
+12VSD -> 12 VOLTS ON ONLY IN RUN MODE (OFF IN SLEEP/SHUTDOWN)
+3,3V -> 3.3 VOLTS ON IN SLEEP/RUN (OFF IN SHUTDOWN)
+5VSD -> 5.0 VOLTS (FOR CALL PROGRESS) ON IN RUN ONLY.
TRICKLE_5V -> 5.0 VOLTS ALWAYS ON.

APPLE COMPUTER INC.

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CR-30

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0029	1	CONN,RCPT,R/A,3.5MMHDPHNE,6.5MM H,NMP,3P	J9	PROJECT	

31 30 29 33 +AUD5V
R425 100K 1% 1/16W MF 603
C350 0.1UF N20P80% 16V CERM 603
R72 100K 1% 1/16W MF 603
U20 TS924 SOI
18 AUDIO_HP_SENSE
HSENSE_NEG
HS_POS
R74 100K 1% 1/16W MF 603
C338 0.1UF N20P80% 16V CERM 603
R426 68.1K 1% 1/16W MF 603
HSENSE
L36 1000-OHM-EMI SM
L30 1000-OHM-EMI SM
INDCAP2
C273 100PF 5% 50V CERM 603

R414 20K 1% 1/16W MF 603
32 29 AOUTL
R413 20K 1% 1/16W MF 603
EOLO
ACOMT
U20 TS924 SOI
DOLO
C57 100UF 20% 6.3V ELEC SM
C77 0.01UF 5% 25V CERM 603
COLO
R407 22 5% 1/16W MF 603
R408 1K 1% 1/16W MF 603
R419 4.75K 1% 1/16W MF 603
HMUTEL
Q2 2N3904 SM
R391 22 5% 1/16W MF 603
BOLO
L37 1000-OHM-EMI SM
L24 1000-OHM-EMI SM
AOLO
INDCAP1
C269 100PF 5% 50V CERM 603
NOSTUFF
R7 10K 1% 1/16W MF 603
514-0029
OMIT
PROJECT
JA1333L-N109
J9
TH
LINE_OUT_COM
LINE_OUT_L
NC_HPJACK5
NO TEST
LINE_OUT_SENSE
LINE_OUT_R

31 30 29 33 +AUD5V
R415 20K 1% 1/16W MF 603
32 29 AOUTR
R417 20K 1% 1/16W MF 603
EORO
ACOMT2
U20 TS924 SOI
DORO
Q1 2N3904 SM
R420 4.75K 1% 1/16W MF 603
HMUTER
R394 1K 1% 1/16W MF 603
C56 100UF 20% 6.3V ELEC SM
CORO
R392 22 5% 1/16W MF 603
R393 22 5% 1/16W MF 603
BORO
AORO
L38 1000-OHM-EMI SM
L32 1000-OHM-EMI SM
INDCAP3
C275 100PF 5% 50V CERM 603
NOSTUFF
R318 10K 1% 1/16W MF 603
D12 SOT23
BAS40-4

TRICKLE_5V INPUT
RAIL WENT FROM 5 TO 12V!!
28 27 23 16 33 28 27 22 +12V_MAIN
R127 10K 1% 1/16W MF 603
R129 33.2K 1% 1/16W MF 603
R122 232 1% 1/16W MF 603
HMUTE_5VR
Q4 2N3906 SM
R130 33.2K 1% 1/16W MF 603
HMUTEI1
R126 33.2K 1% 1/16W MF 603
HMUTEI2
HMUTEI3
HMUTE
29 STARAG6
OMIT
XS2
R75 1 1% 1/4W FF 1210
HEAD_GND
L40 1000-OHM-EMI SM
L22 1000-OHM-EMI SM
INDCAP4
C268 100PF 5% 50V CERM 603

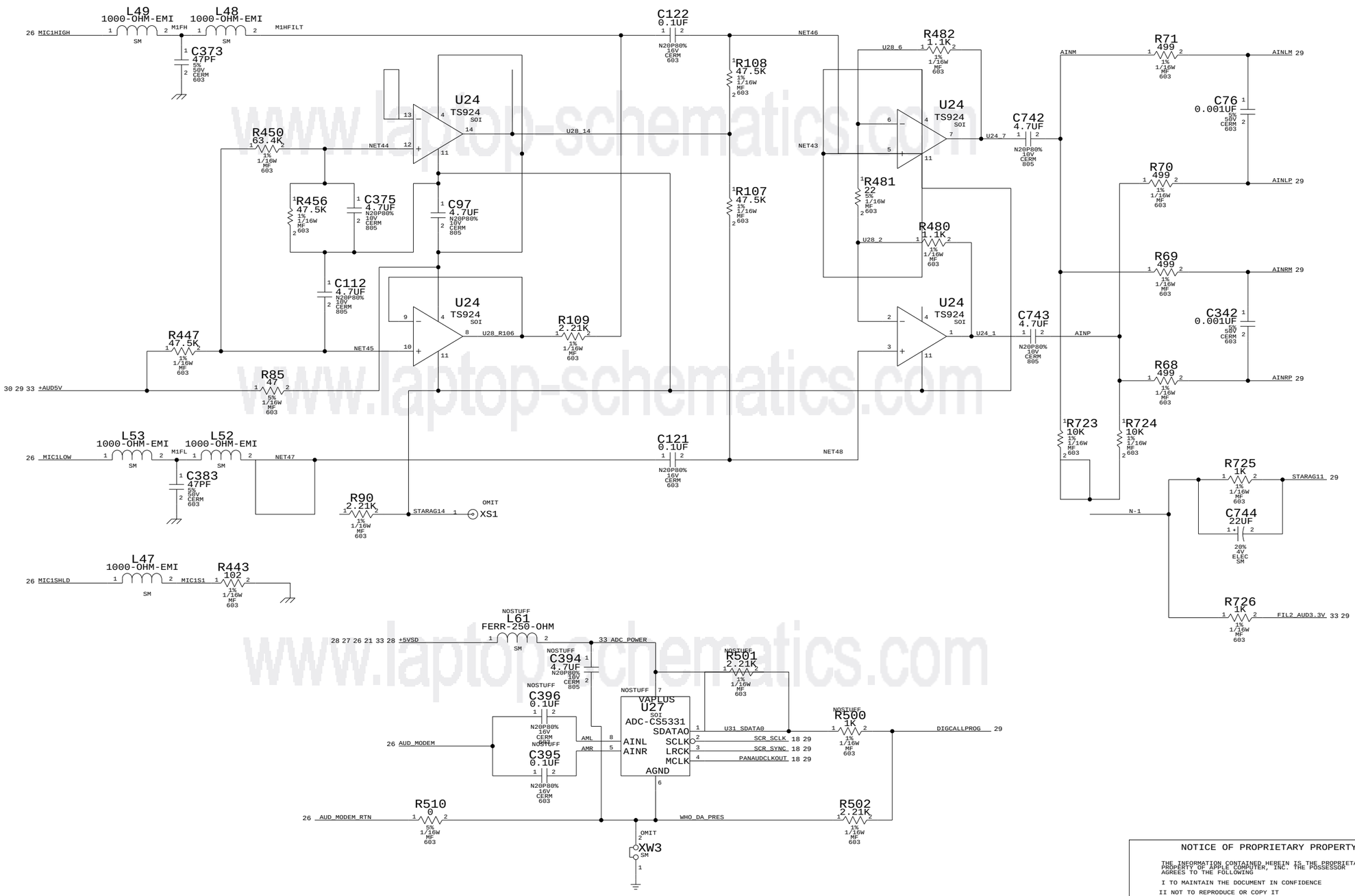
18 AUDIO_HP_MUTE
Q5 2N7002 SM
R128 100K 1% 1/16W MF 603
C130 10UF N20P80% 16V CERM 1206
CHANGED FROM 4.7 TO 10UF
R423 20K 1% 1/16W MF 603
AUD_CHASE
C349 4.7UF N20P80% 10V CERM 805
AUD_CHASC
R432 47 5% 1/16W MF 603
AUD_CHS1
L39 1000-OHM-EMI SM
L23 1000-OHM-EMI SM
INDCAP5
C263 100PF 5% 50V CERM 603
C357 0.01UF 5% 50V CERM 603
R418 47 5% 1/16W MF 603
C331 0.01UF 5% 50V CERM 603

R424 20K 1% 1/16W MF 603
29 ACOM
R433 20K 1% 1/16W MF 603
R427 20K 1% 1/16W MF 603
NET31
C337 4.7UF N20P80% 10V CERM 805
AUD_CHASB

TUMBLER AUDIO, HEADPHONE DRIVER

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6101	12
SCALE: NONE	SHT 30 OF 44	



TUMBLER AUDIO, MICROPHONE PREAMP AND MODEM CALL PROGRESS

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6101 | REV. 12

SCALE NONE | SHT 31 OF 44

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0020	1	CONN,2.5MM PH JACK,RT ANG,6-P,NMP	J7	PROJECT	

SIG_NAME	MIN_LINE_WIDTH	VOLTAGE	MIN_NECK_WIDTH
OUTP1	25		10
OUTP2	25		10
OUTM1	25		10
OUTM2	25		10
OUTP1FILT	25		10
OUTP2FILT	25		10
OUTM1FILT	25		10
OUTM2FILT	25		10
SPKR_L+	25		10
SPKR_L-	25		10
SPKR_R+	25		10
SPKR_R-	25		10

ID ROM V(IL) = 0.5V
RISETIME SENSITIVE; SW PROVIDES 4US INTERBIT GAP

514-0020

TUMBLER AUDIO, POWER AMP.

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6101	12
SCALE: NONE	SHT 32 OF 44	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-6101	1	SCHEM,PCBA,P11	PCB1	
056-0862	1	DESIGN GUIDE	PCB1	
DESIGN IF SPECIAL G3 NEEDED> 056-0928	1	DWG,DSGN GD,MLB,P11	PCB1	OMIT
613-3302	1	GEN DWG, PCBA MECH SUBASSY	PCB1	
820-1257	1	PCBF,MLB,P11	PCB1	

HARDWARE

410-1105	2	WIRELESS CONENCTOR SCREW	J22,J22	
835-0101	2	WIRELESS CONNECTOR NUT	J22,J22	
600-9413	1	HEATSINK,MONICA,REAL	U22	OMIT
730-0231	1	HEATSINK,MONICA,STEALTH	U22	OMIT
730-0214	1	HEATSINK,MICROPROCESSOR	U13	OMIT
730-0202	1	HEATSINK,MICROPROCESSOR	U13	OMIT
730-0217	1	HEATSINK,PANGEA	U6	STEALTH
730-0217	1	HEATSINK,PANGEA	U6	REAL
600-9414	1	HEATSINK,TRIPATH,REAL	U4	OMIT
730-0230	1	HEATSINK,TRIPATH,STEALTH	U4	OMIT
875-0498	1	GAP FILLER VGER CPU	U13	REAL

MODEM/MISC

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
525-0057	1	BATTERY HOLDER	BT1		
825-2029	1	LABEL,SERIAL NUMBER BARCODE	PCB1		
617-0186	1	MODEM, SPRING, W/RJ11	J12	PROJECT	OMIT
617-0201	1	MODEM, DASH, W/RJ11	J12	PROJECT	OMIT
617-0205	1	MODEM, DASH, W/NO RJ11	J12	PROJECT	OMIT
617-0212	1	EMI FILTER PCB,DASH,W/NO RJ11	J12	PROJECT	OMIT
617-0196	1	MODEM, B4, W/NO RJ11	J12	PROJECT	OMIT
617-0196	1	MODEM, AU5, W/NO RJ11	J12	PROJECT	OMIT

617-0196 ALSO REQUIRES DONGLE 611-0138, BUT THAT IS INCLUDED IN ACCESSORY KIT

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
617-0213	1	MODEM, SPRING2, W/NO RJ11	J12	PROJECT	OMIT
617-0212	1	EMI FILTER PCB,SPRING2,W/NO RJ11	J12	PROJECT	OMIT

SODIMMS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333-0336	1	IC,SDRAM,64MB ,PC100,SODIMM	J21	PROJECT	OMIT
333-0360	1	IC,SDRAM,128MB,PC100,SODIMM	J21	PROJECT	OMIT
MICRON> 333-0362	1	IC,SDRAM,256MB,PC100,MICRON,SODIMM	J21	PROJECT	OMIT
SAMSUNG/HUNDAI> 333-0363	1	IC,SDRAM,256MB,PC100,SAM/HYUN,SODIMM	J21	PROJECT	OMIT
333-0364	1	IC,SDRAM,512MB,PC100,SODIMM	J21	PROJECT	OMIT

168 PIN DIMMS

333-0112	1	IC,SDRAM,64MB,PC100,4BK,168P DIMM	J19	PROJECT	OMIT
333-0346	1	IC,SDRAM,128MB,PC100,4BK,168P DIMM	J19	PROJECT	OMIT
333-0347	1	IC,SDRAM,256MB,PC100,4BK,168P DIMM	J19	PROJECT	OMIT
333-0349	1	IC,SDRAM,512MB,PC100,4BK,168P DIMM	J19	PROJECT	OMIT

HOLES AND SLOTS

ZH2 394R177
25 19 33 CHASSIS2 1 OMIT

ZH3 394R177
1 OMIT

I124
ZH1 394R138
1 OMIT

SIG_NAME	MIN_LINE_WIDTH	VOLTAGE	MIN_NECK_WIDTH	
	200	5	10	
	25	3.3	10	
	100	12	10	
	25	0	10	
	25	0	10	
CPUOVDD	25	1.8	10	3 22 24 3 5 13 14 18 20 21
VGER_VCORE	15	2.0	10	22 23 24
+AVDD_CPU	25	2.0	10	3 22 24
L3_OVDD	15	1.5	10	3
L3_CORE	15	2.5	10	4 20 21 22
PANGEA_AVDD5	10	1.8	10	21 4
PANGEA_AVDD4	10	3.3	10	5
+12VSD_FILT	100	12	10	6
AGPVDD	10	3.3	10	26
PANGEA_AVDD6	10	3.3	7	8
AGPVREF	10	1.32	10	8
GRAPH_CORE	25	1.9	10	8 9
+5VSD	100	5	10	22 9
+12VSD	100	12	10	28 21 26 27 28 31
IFP_AVCC	10	3.3	10	26 28 16 26 27
MAINCLK_VDD	25	3.3	10	9
IFP0AVCC	10	3.3	7	7
DACVDD	10	3.3	10	9
FB2_5	25	2.5	10	9
M_VREF1	10	1.25	10	22 10 11
M_VREF2	10	1.25	10	11
PANGEA_AMVDD	10	3.3	10	11
PANGEA_TEI		0	10	13 14
ETH_RXD_PD		0	10	13
GBE_REFCLK		0	10	13
PANGEAVCORE	25	2.5	10	13
VCCA	10	3.3	10	22 13 14
VCCTXFM	10	3.3	10	15
PHYAD		0	10	15
ENET_TST		0	10	15
ENETCNT		0	10	15
PWRDWN		0	10	15
FW_PHY_3_3	10	3.3	10	15
3.8V_TRICKLE	10	3.8	10	16
3.3V_TO_FW	10	3.3	10	16 23 27
G_SSCLK_VDD	25	3.3	10	16
FW_VP_2	40	30	10	12
FW_VP_1	40	30	10	16
FW_VP	40	30	10	16
FW_VGND	40	0	10	16
AUDAMPPOWER	70	12	10	32
12V_LP_FILT	25	12	10	29
12V_FILT	25	12	10	29
J14_10	25	3.3	10	26
LED_RET	25	5	10	26 28
LED_RET_FILT	25	5	10	26
XS_SPKR	70	0	10	32

SIG_NAME	MIN_LINE_WIDTH	VOLTAGE	MIN_NECK_WIDTH	
CHASSIS2	25	0	10	33 19 25
KS5VSD	15	5	10	26
LED_5V	25	5	10	26
LED_5V_FILT	25	5	10	26
PANGEA_VDDA3	10	3.3	7	18
PANGEA_VDDA2	10	3.3	10	18
PANGEA_VDDA1	10	3.3	10	18
VDD_USB	10	3.3	7	18
USB_PWR_AB		3.3	10	
USB_PWR_CD		3.3	10	
USB_PWR_FLT		5	10	19 18
AUD_STAR	10	0	10	33
USB_PWR	200	5	10	19
USB1_PWR	200	5	10	19
USB1_GND	200	0	10	19
USB2_PWR	200	5	10	19
USB2_GND	200	0	10	19
USB3_PWR	200	5	10	19
USB3_GND	200	0	10	19
PMU_POWER	10	3.3	10	23 28 23 28
PMU_AVCC	10	3.3	10	23
+3.3VFPD	25	3.3	10	28 9 25
DDC_VCC_3	10	3.3	10	25
INT_TMDS_3V	10	3.3	10	25
3_5_HONKER	50	3.5	25	28
DETECT_5VT		3.3	10	26
+12V_MAIN	600	12	25	22 27 28 16 23 27 28 30
+12V_DROPPED	50	12	10	23
UIDE_IOCS16_L		5	10	26
+12VSDA	100	12	10	28 29 32
+5VSD_T	40	5	10	27
+12VSD_T	40	12	10	27
+AUD5V	10	5	10	29 30 31
FIL2_DIG3.3V	10	3.3	10	29
ADC_POWER	40	5	10	31
DIG_AUD3.3V	10	3.3	10	29
FIL_AUD3.3V	10	3.3	10	29
+AUD3.3V	15	3.3	10	29
AUD_STAR	15	0	10	33
FIL2_AUD3.3V	10	3.3	10	29 31
AUDAMP5V	10	5	10	32
SPKR_RTN	100	0	10	28 32
DDC_VCC_5	50	0	10	25
FUSED_DDC_5V	50	0	10	25

I/O CONNECTORS

USB	SHEET 18	J2, J3, J5
ETHERNET	SHEET 14	J1
FIREWIRE	SHEET 15	J4, J6
VGA	SHEET 24	J8
HEADPHONE	SHEET 29	J9
MODEM	MODEM SCHEM	MODEM SCHEM
DC IN	SHEET 26	J15
SPKR	SHEET 31	J7

Holes and Slots AND EMC INFO

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6101	12
SCALE: NONE	SHT 33 OF 44	

SIG_NAME	PULSE_PARAM	MAX_VIA_COUNT	NET_SCHED	DELAY_RULE	STUB_LENGTH	NET_SPACING_TYPE	
CPU_DATA<0>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<1>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<2>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<3>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<4>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<5>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<6>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<7>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<8>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<9>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<10>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<11>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<12>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<13>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<14>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<15>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<16>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<17>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<18>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<19>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<20>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<21>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<22>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<23>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<24>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<25>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<26>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<27>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<28>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<29>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<30>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<31>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<32>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<33>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<34>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<35>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<36>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<37>	100000000::	7		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<38>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<39>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<40>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<41>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<42>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<43>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<44>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<45>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<46>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<47>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<48>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<49>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<50>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<51>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<52>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<53>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<54>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<55>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<56>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<57>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<58>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<59>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<60>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<61>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<62>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<63>	100000000::	7		::2000:4500	200		OUT 3 5 24 5 24

SIG_NAME	PULSE_PARAM	MAX_VIA_COUNT	NET_SCHED	DELAY_RULE	STUB_LENGTH	NET_SPACING_TYPE	
KEY PANGEA TIMING CPU_BR*	100000000::	6		::2000:4500			OUT 3 24 5 20
KEY PANGEA TIMING TS*	100000000::	6		::2000:4500			OUT 3 5 24 20
TBST*	100000000::	6		::2000:4500			OUT 3 5 24 20
AACK*	100000000::	6		::2000:4500	200		OUT 5 24 3 20
KEY PANGEA TIMING ARTRY*	100000000::	6		::2000:4500	200		OUT 3 5 24 20
DBWO*	100000000::	6		::2000:4500	200		OUT 5 24 3 20
KEY PANGEA TIMING QREQ*	100000000::	6		::2000:4500	200		OUT 3 24 5 20
QACK*	100000000::	8		::2000:4500	200		OUT 5 24 3
TA*	100000000::	6		::2000:4500	200		OUT 5 24 3 20
TEA*	100000000::	6		::2000:4500	200		OUT 5 24 3 20
TT<0>	100000000::	6		::2000:4500			OUT 3 5 24 20
TT<1>	100000000::	6		::2000:4500			OUT 3 5 24 20
TT<2>	100000000::	6		::2000:4500			OUT 3 5 24 20
TT<3>	100000000::	6		::2000:4500			OUT 3 5 24 20
TT<4>	100000000::	6		::2000:4500			OUT 3 5 24 20
TSIZ<0>	100000000::	6		::2000:4500	200		OUT 3 5 24
TSIZ<1>	100000000::	6		::2000:4500	200		OUT 3 5 24
TSIZ<2>	100000000::	6		::2000:4500	200		OUT 3 5 24
CPU_ADDR<0>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
CPU_ADDR<1>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
CPU_ADDR<2>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
CPU_ADDR<3>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
CPU_ADDR<4>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
CPU_ADDR<5>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
CPU_ADDR<6>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
CPU_ADDR<7>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
CPU_ADDR<8>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
CPU_ADDR<9>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
CPU_ADDR<10>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
CPU_ADDR<11>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
CPU_ADDR<12>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
CPU_ADDR<13>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
CPU_ADDR<14>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
CPU_ADDR<15>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
CPU_ADDR<16>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
CPU_ADDR<17>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
CPU_ADDR<18>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
CPU_ADDR<19>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
CPU_ADDR<20>	100000000::	6		::2000:4500	220		OUT 3 5 24 3 5 24
CPU_ADDR<21>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
CPU_ADDR<22>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
CPU_ADDR<23>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
CPU_ADDR<24>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
CPU_ADDR<25>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
CPU_ADDR<26>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
CPU_ADDR<27>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
CPU_ADDR<28>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
CPU_ADDR<29>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
CPU_ADDR<30>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
CPU_ADDR<31>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
GBL*	100000000::	6		::2000:4500			OUT 3 5 24 20
CPU_DBG*	100000000::	6		::2000:4500			OUT 5 24 3 20
CPU_BG*	100000000::	6		::2000:4500	200		OUT 3 5 24 20
WT*	100000000::	6		::2000:4500	200		OUT 3 5 24 20
CI*	100000000::	6		::2000:4500	210		OUT 3 5 24 20

CONSTRAINTS -- CPU BUS

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6101 | REV. 12

SCALE NONE | SHT 34 OF 44

SIG_NAME	PULSE_PARAM	MAX_VIA_COUNT	DELAY_RULE	STUB_LENGTH	NET_SPACING_TYPE	NET_SCHED
MDATA<0>	100000000::	6	::1850:4400	200		U6.AG1 J21.3 J19.2
MDATA<1>	100000000::	6	::1850:4400	200		U6.AF3 J21.5 J19.3
MDATA<2>	100000000::	6	::1850:4400	200		U6.AF1 J21.7 J19.4
MDATA<3>	100000000::	6	::1850:4400	200		U6.AE2 J21.9 J19.5
MDATA<4>	100000000::	6	::1850:4400	200		U6.AE1 J21.13 J19.7
MDATA<5>	100000000::	6	::1850:4400	200		U6.AD2 J21.15 J19.8
MDATA<6>	100000000::	6	::1850:4400	200		U6.AD1 J21.17 J19.9
MDATA<7>	100000000::	6	::1850:4400	200		U6.AC2 J21.19 J19.10
MDATA<8>	100000000::	6	::1850:4400	200		U6.Y1 J21.37 J19.11
MDATA<9>	100000000::	6	::1850:4400	200		U6.Y2 J21.39 J19.13
MDATA<10>	100000000::	6	::1850:4400	200		U6.W1 J21.41 J19.14
MDATA<11>	100000000::	6	::1850:4400	200		U6.W2 J21.43 J19.15
MDATA<12>	100000000::	6	::1850:4400	200		U6.V2 J21.47 J19.16
MDATA<13>	100000000::	6	::1850:4400	200		U6.U2 J21.49 J19.17
MDATA<14>	100000000::	6	::1850:4400	200		U6.T1 J21.51 J19.19
MDATA<15>	100000000::	6	::1850:4400	200		U6.T2 J21.53 J19.20
MDATA<16>	100000000::	6	::1850:4400	200		U6.R1 J21.83 J19.55
MDATA<17>	100000000::	6	::1850:4400	200		U6.R2 J21.85 J19.56
MDATA<18>	100000000::	6	::1850:4400	200		U6.P3 J21.87 J19.57
MDATA<19>	100000000::	6	::1850:4400	200		U6.P2 J21.89 J19.58
MDATA<20>	100000000::	6	::1850:4400	200		U6.N1 J21.93 J19.60
MDATA<21>	100000000::	6	::1850:4400	200		U6.N2 J21.95 J19.65
MDATA<22>	100000000::	6	::1850:4400	200		U6.M1 J21.97 J19.66
MDATA<23>	100000000::	6	::1850:4400	200		U6.M2 J21.99 J19.67
MDATA<24>	100000000::	6	::1850:4400	200		U6.J2 J21.121 J19.69
MDATA<25>	100000000::	6	::1850:4400	200		U6.H2 J21.123 J19.70
MDATA<26>	100000000::	6	::1850:4400	200		U6.G1 J21.125 J19.71
MDATA<27>	100000000::	6	::1850:4400	200		U6.G2 J21.127 J19.72
MDATA<28>	100000000::	6	::1850:4400	200		U6.F1 J21.131 J19.74
MDATA<29>	100000000::	6	::1850:4400	200		U6.F2 J21.133 J19.75
MDATA<30>	100000000::	6	::1850:4400	200		U6.E1 J21.135 J19.76
MDATA<31>	100000000::	6	::1850:4400	200		U6.H3 J21.137 J19.77
MDATA<32>	100000000::	6	::1850:4400	200		U6.AD3 J21.4 J19.86
MDATA<33>	100000000::	6	::1850:4400	200		U6.AD5 J21.6 J19.87
MDATA<34>	100000000::	6	::1850:4400	200		U6.AC3 J21.8 J19.88
MDATA<35>	100000000::	6	::1850:4400	200		U6.AC5 J21.10 J19.89
MDATA<36>	100000000::	6	::1850:4400	200		U6.AC6 J21.14 J19.91
MDATA<37>	100000000::	6	::1850:4400	200		U6.AC7 J21.16 J19.92
MDATA<38>	100000000::	6	::1850:4400	200		U6.AB6 J21.18 J19.93
MDATA<39>	100000000::	6	::1850:4400	200		U6.AB7 J21.20 J19.94
MDATA<40>	100000000::	6	::1850:4400	200		U6.AA5 J21.38 J19.95
MDATA<41>	100000000::	6	::1850:4400	200		U6.AA6 J21.40 J19.97
MDATA<42>	100000000::	6	::1850:4400	200		U6.AA7 J21.42 J19.98
MDATA<43>	100000000::	6	::1850:4400	200		U6.AC1 J21.44 J19.99
MDATA<44>	100000000::	6	::1850:4400	200		U6.V3 J21.48 J19.100
MDATA<45>	100000000::	6	::1850:4400	200		U6.V5 J21.50 J19.101
MDATA<46>	100000000::	6	::1850:4400	200		U6.V6 J21.52 J19.103
MDATA<47>	100000000::	6	::1850:4400	200		U6.W7 J21.54 J19.104
MDATA<48>	100000000::	6	::1850:4400	200		U6.U3 J21.84 J19.139
MDATA<49>	100000000::	6	::1850:4400	200		U6.U5 J21.86 J19.140
MDATA<50>	100000000::	6	::1850:4400	200		U6.U6 J21.88 J19.141
MDATA<51>	100000000::	6	::1850:4400	200		U6.U7 J21.90 J19.142
MDATA<52>	100000000::	6	::1850:4400	200		U6.R6 J21.94 J19.144
MDATA<53>	100000000::	6	::1850:4400	200		U6.R7 J21.96 J19.149
MDATA<54>	100000000::	6	::1850:4400	200		U6.P5 J21.98 J19.150
MDATA<55>	100000000::	6	::1850:4400	200		U6.P6 J21.100 J19.151
MDATA<56>	100000000::	6	::1850:4400	200		U6.L6 J21.122 J19.153
MDATA<57>	100000000::	6	::1850:4400	200		U6.L7 J21.124 J19.154
MDATA<58>	100000000::	6	::1850:4400	200		U6.K6 J21.126 J19.155
MDATA<59>	100000000::	6	::1850:4400	200		U6.K7 J21.128 J19.156
MDATA<60>	100000000::	6	::1850:4400	200		U6.J3 J21.132 J19.158
MDATA<61>	100000000::	6	::1850:4400	200		U6.J5 J21.134 J19.159
MDATA<62>	100000000::	6	::1850:4400	200		U6.J6 J21.136 J19.160
MDATA<63>	100000000::	6	::1850:4400	200		U6.J7 J21.138 J19.161

SIG_NAME	PULSE_PARAM	MAX_VIA_COUNT	MIN_LINE_WIDTH	NET_SCHED	DELAY_RULE	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE
PANGEAMCLK<1>	100000000::	3	6		::1800:2000		100	10 MIL SPACING
PANGEAMCLK<3>	100000000::	3	6		::1800:2000		100	10 MIL SPACING
PANGEAMCLK<4>	100000000::	3	6		::1800:2000		100	10 MIL SPACING
PANGEAMCLK<5>	100000000::	3	6		::1800:2000		100	10 MIL SPACING
PANGEAMCLK<6>	100000000::	3	6		::1800:2000		100	10 MIL SPACING
PANGEAMCLK<7>	100000000::	3	6		::1800:2000		100	10 MIL SPACING
MAINCLK_XIN	100000000::				::1800:2000			10 MIL SPACING
MAINCLK_XOUT	100000000::				::1800:2000			10 MIL SPACING
MCLK<1>	100000000::	4	6	J21.74 R550.2 R680.2	::2000:3500	250		10 MIL SPACING
MCLK<3>	100000000::	4	6	J21.61 R556.2 R668.2	::2000:3500	250		10 MIL SPACING
MCLK<4>	100000000::	4	6	J19.42 R547.2 R560.2	::2000:3500	250		10 MIL SPACING
MCLK<5>	100000000::	4	6	J19.125 R543.2 R580.2	::2000:3500	250		10 MIL SPACING
MCLK<6>	100000000::	4	6	J19.79 R558.2 R572.2	::2000:4500	250		10 MIL SPACING
MCLK<7>	100000000::	4	6	J19.163 R552.2 R656.2	::2000:4500	250		10 MIL SPACING
MCLKOUT<1>	100000000::	2	6		:::250			10 MIL SPACING
MCLKOUT<3>	100000000::	2	6		:::250			10 MIL SPACING
MCLKOUT<4>	100000000::	2	6		:::250			10 MIL SPACING
MCLKOUT<5>	100000000::	2	6		:::250			10 MIL SPACING
MCLKOUT<6>	100000000::	2	6		:::250			10 MIL SPACING
MCLKOUT<7>	100000000::	2	6		:::250			10 MIL SPACING
M_ADDR<0>	100000000::	4			::400:1200		200	
M_ADDR<1>	100000000::	4			::400:1200		200	
M_ADDR<2>	100000000::	4			::400:1200		200	
M_ADDR<3>	100000000::	4			::400:1200		200	
M_ADDR<4>	100000000::	4			::400:1200		200	
M_ADDR<5>	100000000::	4			::400:1200		200	
M_ADDR<6>	100000000::	4			::400:1200		200	
M_ADDR<7>	100000000::	4			::400:1200		200	
M_ADDR<8>	100000000::	4			::400:1200		200	
M_ADDR<9>	100000000::	4			::400:1200		200	
M_ADDR<10>	100000000::	4			::400:1200		200	
M_ADDR<11>	100000000::	4			::400:1200		200	
M_ADDR<12>	100000000::	4			::400:1200		200	
TERM_M_ADDR<0>	100000000::	8		RP33.2 J21.29 RP29.8	::1100:3200			
TERM_M_ADDR<1>	100000000::	8		RP9.4 J21.31 RP29.7	::1100:3200			
TERM_M_ADDR<2>	100000000::	8		RP31.1 J21.33 RP26.6	::1100:3200			
TERM_M_ADDR<3>	100000000::	8		6RP9.3 J21.30 RP26.5	::1100:3200			
TERM_M_ADDR<4>	100000000::	8		RP31.2 J21.32 RP26.8	::1100:3200			
TERM_M_ADDR<5>	100000000::	8		RP9.1 J21.34 RP26.7	::1100:3300			
TERM_M_ADDR<6>	100000000::	8		RP21.1 J21.103 RP24.6	::1100:3200			
TERM_M_ADDR<7>	100000000::	8		RP23.2 J21.104 RP24.5	::1100:3200			
TERM_M_ADDR<8>	100000000::	8		RP21.2 J21.105 RP24.8				
TERM_M_ADDR<9>	100000000::	8		RP21.3 J21.109 RP24.7				
TERM_M_ADDR<10>	100000000::	8		RP21.4 J21.111 RP22.6	::1050:3200			
TERM_M_ADDR<11>	100000000::	8		RP23.3 J21.112 RP22.7	::1100:3200			
TERM_M_ADDR<12>	100000000::	8		R540.2 J21.70 R123.1				

CONSTRAINTS -- MEMORY PAGE 1

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6101 | REV. 12

SCALE NONE | SHT 35 OF 44

CR-36

SIG_NAME	PULSE_PARAM	MAX_VIA_COUNT	DELAY_RULE	STUB_LENGTH	NET_SPACING_TYPE	NET_SCHED	
T_M_BA0	100MHZ::	5	::1100:2400	200	5 MIL SPACING	RP23.1 J21.106 RP22.5	OUT 6
T_M_BA1	100MHZ::	5	::1100:2400		5 MIL SPACING	RP23.4 J21.110 RP22.8	OUT 6
T_SDRAS*	100MHZ::	5			5 MIL SPACING	RP31.4 J21.65 RP29.6	OUT 6
T_SDCAS*	100MHZ::	5	::1100:2400	200	5 MIL SPACING	RP31.3 J21.66 RP29.5	OUT 6
T_MEMWE*	100MHZ::	5	::1100:2400	200	5 MIL SPACING	R539.1 J21.67 R158.2	OUT 6
T2_M_BA0	100MHZ::	4	::100:500	200	5 MIL SPACING		OUT 6
T2_M_BA1	100MHZ::	4	::100:500	200	5 MIL SPACING		OUT 6
T2_SDRAS*	100MHZ::	4	::100:500	200	5 MIL SPACING		OUT 6
T2_SDCAS*	100MHZ::	4	::100:840	200	5 MIL SPACING		OUT 6
T2_MEMWE*	100MHZ::	4	::100:500	200	5 MIL SPACING		OUT 6

SIG_NAME	PULSE_PARAM	MIN LINE_WIDTH MAX_VIA_COUNT		NET_SCHED	DELAY_RULE	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	
PANGEA_CPU_CLK	100MHZ::	2	6		::300:500		100	10 MIL SPACING	OUT 5
CPU_CLK	100MHZ::	6	6		::2700:4100	1000	200	10 MIL SPACING	OUT 3 5 7
CPUFBOUT	100MHZ::	2	6		::100:600		100	10 MIL SPACING	OUT 5
TCPUFBOUT	100MHZ::	2	6		::475:700		100	10 MIL SPACING	OUT 5 7
CPUFB7	100MHZ::	2	6		::2700:3000		100	10 MIL SPACING	OUT 5
CPUFB6	100MHZ::	2	6		::1800:2000		100	10 MIL SPACING	OUT 5
CPUFB5	100MHZ::	2	6		::1800:2000		100	10 MIL SPACING	OUT 5
CPUFB4	100MHZ::	2	6		::1800:2000		100	10 MIL SPACING	OUT 5
CPUFB3	100MHZ::	2	6		::1800:2000		100	10 MIL SPACING	OUT 5
CPUFB2	100MHZ::	2	6		::1800:2000		100	10 MIL SPACING	OUT 5
CPUFB1	100MHZ::	2	6		::2600:3000		100	10 MIL SPACING	OUT 5
CPUFBIN	100MHZ::	6	6		::475:1300	1000	100	10 MIL SPACING	OUT 5 7
AGPFB0	66MHZ::	2	5		::950:1000	250	100	10 MIL SPACING	OUT 8
AGPFB1	66MHZ::	2	5		::475:700		100	10 MIL SPACING	OUT 8
AGPFB2	66MHZ::	2	5		::950:1100		100	10 MIL SPACING	OUT 8
AGPFB3	66MHZ::	2	5		::475:700		100	10 MIL SPACING	OUT 8
SCHMOO_CPU_CLK	100MHZ::	2	6		::300:500	250	100	10 MIL SPACING	OUT
BANDAID	18.432MHZ::	3			:::2700		100	10 MIL SPACING	OUT

SIG_NAME	PULSE_PARAM	MAX_VIA_COUNT	NET_SCHED	DELAY_RULE	STUB_LENGTH	NET_SPACING_TYPE	
TERM2_M_ADDR<0>	100MHZ::	4		::100:500	200	5 MIL SPACING	OUT 6 8 6 8
TERM2_M_ADDR<1>	100MHZ::	4		::100:500	200	5 MIL SPACING	OUT 6 8 6 8
TERM2_M_ADDR<2>	100MHZ::	4		::100:500	200	5 MIL SPACING	OUT 6 8 6 8
TERM2_M_ADDR<3>	100MHZ::	4		::100:500	200	5 MIL SPACING	OUT 6 8 6 8
TERM2_M_ADDR<4>	100MHZ::	4		::100:500	200	5 MIL SPACING	OUT 6 8 6 8
TERM2_M_ADDR<5>	100MHZ::	4		::100:500	200	5 MIL SPACING	OUT 6 8 6 8
TERM2_M_ADDR<6>	100MHZ::	4		::100:500	200	5 MIL SPACING	OUT 6 8 6 8
TERM2_M_ADDR<7>	100MHZ::	4		::100:500	200	5 MIL SPACING	OUT 6 8 6 8
TERM2_M_ADDR<8>	100MHZ::	4		::100:500	200	5 MIL SPACING	OUT 6 8 6 8
TERM2_M_ADDR<9>	100MHZ::	4		::100:500	200	5 MIL SPACING	OUT 6 8 6 8
TERM2_M_ADDR<10>	100MHZ::	4		::100:700	200	5 MIL SPACING	OUT 6 8 6 8
TERM2_M_ADDR<11>	100MHZ::	4		::100:700	200	5 MIL SPACING	OUT 6 8 6 8
TERM2_M_ADDR<12>	100MHZ::	4		::100:700	200	5 MIL SPACING	OUT 6 8 6 8
DQM0*	100MHZ::	4		::3000:4000	200	5 MIL SPACING	OUT 6
DQM1*	100MHZ::	4		::3000:4000	200	5 MIL SPACING	OUT 6
DQM2*	100MHZ::	4		::3000:4000	200	5 MIL SPACING	OUT 6
DQM3*	100MHZ::	4		::3000:4000	200	5 MIL SPACING	OUT 6
DQM4*	100MHZ::	4		::3000:4000	200	5 MIL SPACING	OUT 6
DQM5*	100MHZ::	4		::3000:4000	200	5 MIL SPACING	OUT 6
DQM6*	100MHZ::	4		::3000:4000	200	5 MIL SPACING	OUT 6
DQM7*	100MHZ::	4		::3000:4000	200	5 MIL SPACING	OUT 6
CS0*	100MHZ::	5		::600:1100	200	5 MIL SPACING	OUT 6
CS1*	100MHZ::	5		::600:1100	200	5 MIL SPACING	OUT 6
CS2*	100MHZ::	5		::600:1100	200	5 MIL SPACING	OUT 6
CS3*	100MHZ::	5		::600:1100	200	5 MIL SPACING	OUT 6
T1CS0*	100MHZ::	4		::300:1400	200	5 MIL SPACING	OUT 6
T1CS1*	100MHZ::	4		::300:1400	200	5 MIL SPACING	OUT 6
T2CS2*	100MHZ::	4		::300:2400	200	5 MIL SPACING	OUT 6
T2CS3*	100MHZ::	4		::300:2400	200	5 MIL SPACING	OUT 6
M_BA0	100MHZ::	4		::400:1400	200	5 MIL SPACING	OUT 6
M_BA1	100MHZ::	4		::400:1400	200	5 MIL SPACING	OUT 6
SDRAS*	100MHZ::	4		::400:1000	200	5 MIL SPACING	OUT 6
SDCAS*	100MHZ::	4		::400:1000	200	5 MIL SPACING	OUT 6
MEMWE*	100MHZ::	4		::400:1000	200	5 MIL SPACING	OUT 6

CONSTRAINTS -- MEMORY PAGE 2

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6101	12

SCALE	SHT	OF
NONE	36	44

CONSTRAINTS -- AGP, FIREWIRE, PARTIAL GRAPHICS (1 OF 2)

AGP RELATED DOO-DAHS

SIG_NAME	PULSE_PARAM / MAX_VIA_COUNT	MAX_EXPOSED_LENGTH / STUB_LENGTH	NET_SCHED	NET_SPACING_TYPE	DELAY_RULE	MIN_LINE_WIDTH	
PANGEA_AGP_CLK	66MHZ:: / 3	250 /		10 MIL SPACING	::0225:0275	5	OUT 8
AGP_CLK	66MHZ:: / 12	/		20 MIL SPACING	::3800:3900		OUT 8 9
AGP_FB_IN	66MHZ:: / 3	/		10 MIL SPACING	::1325:1350	5	OUT 8
AGP_FB_OUT	66MHZ:: / 3	/		10 MIL SPACING	::0320:0335	5	OUT 8
AGPCBE<3>	66MHZ:: / 8	/		5 MIL SPACING	::3750:4000		OUT 8 9
AGPCBE<2>	66MHZ:: / 8	/		5 MIL SPACING	::3750:4000		OUT 8 9
AGPCBE<1>	66MHZ:: / 8	/		5 MIL SPACING	::3050:3300		OUT 8 9
AGPCBE<0>	66MHZ:: / 8	/		5 MIL SPACING	::3050:3300		OUT 8 9
AGPAD<31>	66MHZ:: / 8	/		5 MIL SPACING	::3750:4000		OUT 8 9
AGPAD<30>	66MHZ:: / 8	/		5 MIL SPACING	::3750:4000		OUT 8 9
AGPAD<29>	66MHZ:: / 8	/		5 MIL SPACING	::3750:4000		OUT 8 9
AGPAD<28>	66MHZ:: / 8	/		5 MIL SPACING	::3750:4000		OUT 8 9
AGPAD<27>	66MHZ:: / 8	/		5 MIL SPACING	::3750:4000		OUT 8 9
AGPAD<26>	66MHZ:: / 8	/		5 MIL SPACING	::3750:4000		OUT 8 9
AGPAD<25>	66MHZ:: / 8	/		5 MIL SPACING	::3750:4000		OUT 8 9
AGPAD<24>	66MHZ:: / 8	/		5 MIL SPACING	::3750:4000		OUT 8 9
AGPAD<23>	66MHZ:: / 8	/		5 MIL SPACING	::3750:4000		OUT 8 9
AGPAD<22>	66MHZ:: / 8	/		5 MIL SPACING	::3750:4000		OUT 8 9
AGPAD<21>	66MHZ:: / 8	/		5 MIL SPACING	::3750:4000		OUT 8 9
AGPAD<20>	66MHZ:: / 8	/		5 MIL SPACING	::3750:4000		OUT 8 9
AGPAD<19>	66MHZ:: / 8	/		5 MIL SPACING	::3750:4000		OUT 8 9
AGPAD<18>	66MHZ:: / 8	/		5 MIL SPACING	::3750:4000		OUT 8 9
AGPAD<17>	66MHZ:: / 8	/		5 MIL SPACING	::3750:4000		OUT 8 9
AGPAD<16>	66MHZ:: / 8	/		5 MIL SPACING	::3750:4000		OUT 8 9
AGPAD<15>	66MHZ:: / 8	/		5 MIL SPACING	::3050:3300		OUT 8 9
AGPAD<14>	66MHZ:: / 8	/		5 MIL SPACING	::3050:3300		OUT 8 9
AGPAD<13>	66MHZ:: / 8	/		5 MIL SPACING	::3050:3300		OUT 8 9
AGPAD<12>	66MHZ:: / 8	/		5 MIL SPACING	::3050:3300		OUT 8 9
AGPAD<11>	66MHZ:: / 8	/		5 MIL SPACING	::3050:3300		OUT 8 9
AGPAD<10>	66MHZ:: / 8	/		5 MIL SPACING	::3050:3300		OUT 8 9
AGPAD<9>	66MHZ:: / 8	/		5 MIL SPACING	::3050:3300		OUT 8 9
AGPAD<8>	66MHZ:: / 8	/		5 MIL SPACING	::3050:3300		OUT 8 9
AGPAD<7>	66MHZ:: / 8	/		5 MIL SPACING	::3050:3300		OUT 8 9
AGPAD<6>	66MHZ:: / 8	/		5 MIL SPACING	::3050:3300		OUT 8 9
AGPAD<5>	66MHZ:: / 8	/		5 MIL SPACING	::3050:3300		OUT 8 9
AGPAD<4>	66MHZ:: / 8	/		5 MIL SPACING	::3050:3300		OUT 8 9
AGPAD<3>	66MHZ:: / 8	/		5 MIL SPACING	::3050:3300		OUT 8 9
AGPAD<2>	66MHZ:: / 8	/		5 MIL SPACING	::3050:3300		OUT 8 9
AGPAD<1>	66MHZ:: / 8	/		5 MIL SPACING	::3050:3300		OUT 8 9
AGPAD<0>	66MHZ:: / 8	/		5 MIL SPACING	::3050:3300		OUT 8 9
PAN_AGPADSTB<1>	66MHZ:: / 4	250 / 200		10 MIL SPACING	::0500:0550		OUT 8
AGPADSTB<1>	66MHZ:: / 8	/ 200		10 MIL SPACING	::3450:3500		OUT 8 9 20
PAN_AGPADSTB<0>	66MHZ:: / 4	250 / 200		10 MIL SPACING	::0600:0650		OUT 8
AGPADSTB<0>	66MHZ:: / 8	/ 200		10 MIL SPACING	::2650:2700		OUT 8 9 20
AGPST<2>	66MHZ:: / 8	/		5 MIL SPACING	::3500:4500		OUT 8 9 20
AGPST<1>	66MHZ:: / 8	/		5 MIL SPACING	::3500:4500		OUT 8 9 20
AGPST<0>	66MHZ:: / 8	/		5 MIL SPACING	::3500:4500		OUT 8 9 20
AGPREQ*	66MHZ:: / 8	/		5 MIL SPACING	::3500:4500		OUT 9 8 20
AGPGNT*	66MHZ:: / 8	/		5 MIL SPACING	::3500:4500		OUT 8 9 20
AGPPAR	66MHZ:: / 8	/		5 MIL SPACING	::3500:4500		OUT 8 9
AGPFRAME*	66MHZ:: / 8	/		5 MIL SPACING	::3500:4500		OUT 8 9 20
AGPTRDY*	66MHZ:: / 8	/		5 MIL SPACING	::3500:4500		OUT 8 9 20
AGPIRDY*	66MHZ:: / 8	/		5 MIL SPACING	::3500:4500		OUT 8 9 20
PCISTOP*	66MHZ:: / 8	/		5 MIL SPACING	::3500:4500		OUT 8 9 20
AGPDEVSEL*	66MHZ:: / 8	/		5 MIL SPACING	::3500:4500		OUT 8 9 20
AGPPIPE*	66MHZ:: / 8	/		5 MIL SPACING	::3500:4500		OUT 9 8 20
AGPRBF*	66MHZ:: / 8	/		5 MIL SPACING	::3500:4500		OUT 9 8 20

FIREWIRE RELATED DOO-DAHS

SIG_NAME	PULSE_PARAM / MAX_VIA_COUNT	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	DELAY_RULE	
FW_XI	24.576MHZ / 2	250	200	10 MIL SPACING		OUT 16
FW_XO	24.576MHZ / 2	250	200	10 MIL SPACING		OUT 16
FW_SCLK	49.152MHZ / 4	250	200	10 MIL SPACING	::5400:6200	OUT 13 16
FW_PHY_SCLK	49.152MHZ / 2	250	200	10 MIL SPACING	::0100:0300	OUT 16
FW_LINK_D<7>	49.152MHZ / 2		200	5 MIL SPACING	::0500:0800	OUT 13
FW_LINK_D<6>	49.152MHZ / 2		200	5 MIL SPACING	::0500:0800	OUT 13
FW_LINK_D<5>	49.152MHZ / 2		200	5 MIL SPACING	::0500:0800	OUT 13
FW_LINK_D<4>	49.152MHZ / 2		200	5 MIL SPACING	::0500:0800	OUT 13
FW_LINK_D<3>	49.152MHZ / 2		200	5 MIL SPACING	::0500:0800	OUT 13
FW_LINK_D<2>	49.152MHZ / 2		200	5 MIL SPACING	::0500:0800	OUT 13
FW_LINK_D<1>	49.152MHZ / 2		200	5 MIL SPACING	::0500:0800	OUT 13
FW_LINK_D<0>	49.152MHZ / 2		200	5 MIL SPACING	::0500:0800	OUT 13
FW_LINK_CNTL1	49.152MHZ / 2		200	5 MIL SPACING	::0500:0800	OUT 13
FW_LINK_CNTL0	49.152MHZ / 2		220	5 MIL SPACING	::0500:0800	OUT 13
FW_LINK_LREQ	49.152MHZ / 2		200	5 MIL SPACING	::0500:0800	OUT 13
FW_D<7>	49.152MHZ / 4		200	5 MIL SPACING	::4900:5400	OUT 13 16
FW_D<6>	49.152MHZ / 4		200	5 MIL SPACING	::4900:5400	OUT 13 16
FW_D<5>	49.152MHZ / 4		200	5 MIL SPACING	::4900:5400	OUT 13 16
FW_D<4>	49.152MHZ / 4		200	5 MIL SPACING	::4900:5400	OUT 13 16
FW_D<3>	49.152MHZ / 4		200	5 MIL SPACING	::4900:5400	OUT 13 16
FW_D<2>	49.152MHZ / 4		200	5 MIL SPACING	::4900:5400	OUT 13 16
FW_D<1>	49.152MHZ / 4		200	5 MIL SPACING	::4900:5400	OUT 13 16
FW_D<0>	49.152MHZ / 4		200	5 MIL SPACING	::4900:5400	OUT 13 16
FW_CNTL1	49.152MHZ / 4		200	5 MIL SPACING	::4900:5400	OUT 13 16
FW_CNTL0	49.152MHZ / 4		220	5 MIL SPACING	::4900:5400	OUT 13 16
FW_LREQ	49.152MHZ / 4		200	5 MIL SPACING	::5000:5700	OUT 13 16
FW_PHY_D<7>	49.152MHZ / 2		200	5 MIL SPACING	::0100:0300	OUT 16
FW_PHY_D<6>	49.152MHZ / 2		200	5 MIL SPACING	::0100:0300	OUT 16
FW_PHY_D<5>	49.152MHZ / 2		200	5 MIL SPACING	::0100:0300	OUT 16
FW_PHY_D<4>	49.152MHZ / 2		200	5 MIL SPACING	::0100:0300	OUT 16
FW_PHY_D<3>	49.152MHZ / 2		200	5 MIL SPACING	::0100:0300	OUT 16
FW_PHY_D<2>	49.152MHZ / 2		200	5 MIL SPACING	::0100:0300	OUT 16
FW_PHY_D<1>	49.152MHZ / 2		200	5 MIL SPACING	::0100:0300	OUT 16
FW_PHY_D<0>	49.152MHZ / 2		200	5 MIL SPACING	::0100:0300	OUT 16
FW_PHY_CNTL1	49.152MHZ / 2		200	5 MIL SPACING	::0100:0300	OUT 16
FW_PHY_CNTL0	49.152MHZ / 2		200	5 MIL SPACING	::0100:0300	OUT 16

FIREWIRE DIFFERENTIAL THINGIES

SIG_NAME	PULSE_PARAM / MAX_VIA_COUNT	MAX_EXPOSED_LENGTH	NET_SPACING_TYPE	ECL	DIFFERENTIAL_PAIR	
FW_TPB2P	400MHZ / 3		5 MIL SPACING	TRUE	FW_TPB2X	OUT 16
FW_TPB2N	400MHZ / 3		5 MIL SPACING	TRUE	FW_TPB2X	OUT 16
FW_TPA2P	400MHZ / 2		5 MIL SPACING	TRUE	FW_TPA2X	OUT 16
FW_TPA2N	400MHZ / 2		5 MIL SPACING	TRUE	FW_TPA2X	OUT 16
FW_TPB1P	400MHZ / 2		5 MIL SPACING	TRUE	FW_TPB1X	OUT 16
FW_TPB1N	400MHZ / 2		5 MIL SPACING	TRUE	FW_TPB1X	OUT 16
FW_TPA1P	400MHZ / 2		5 MIL SPACING	TRUE	FW_TPA1X	OUT 16
FW_TPA1N	400MHZ / 2		5 MIL SPACING	TRUE	FW_TPA1X	OUT 16
FW_TPI2P	400MHZ / 2		5 MIL SPACING	TRUE	FW_TPI2	OUT 16
FW_TPI2N	400MHZ / 2		5 MIL SPACING	TRUE	FW_TPI2	OUT 16
FW_TPO2P	400MHZ / 2		5 MIL SPACING	TRUE	FW_TPO2	OUT 16
FW_TPO2N	400MHZ / 2		5 MIL SPACING	TRUE	FW_TPO2	OUT 16
FW_TPI1P	400MHZ / 2		5 MIL SPACING	TRUE	FW_TPI1	OUT 16
FW_TPI1N	400MHZ / 2		5 MIL SPACING	TRUE	FW_TPI1	OUT 16
FW_TPO1P	400MHZ / 2		5 MIL SPACING	TRUE	FW_TPO1	OUT 16
FW_TPO1N	400MHZ / 2		5 MIL SPACING	TRUE	FW_TPO1	OUT 16

GRAPHICS DIFFERENTIAL THINGIES

SIG_NAME	PULSE_PARAM / MAX_VIA_COUNT	MAX_EXPOSED_LENGTH	NET_SPACING_TYPE	ECL	DIFFERENTIAL_PAIR	DELAY_RULE	RATSNET_SCHEDULE	
INT_TMDS_D2P	300MHZ:: / 2		10 MIL SPACING		INT_TMDS_D2	::900:1200		OUT 9 25
INT_TMDS_D2M	300MHZ:: / 2		10 MIL SPACING		INT_TMDS_D2	::900:1200		OUT 9 25
INT_TMDS_D1P	300MHZ:: / 2		10 MIL SPACING		INT_TMDS_D1	::900:1200		OUT 9 25
INT_TMDS_D1M	300MHZ:: / 2		10 MIL SPACING		INT_TMDS_D1	::900:1200		OUT 9 25
INT_TMDS_D0P	300MHZ:: / 2		10 MIL SPACING		INT_TMDS_D0	::900:1200		OUT 9 25
INT_TMDS_D0M	300MHZ:: / 2		10 MIL SPACING		INT_TMDS_D0	::900:1200		OUT 9 25
INT_TMDS_CKP	300MHZ:: / 2		10 MIL SPACING		INT_TMDS_CK	::900:1200		OUT 9 25
INT_TMDS_CKM	300MHZ:: / 2		10 MIL SPACING		INT_TMDS_CK	::900:1200		OUT 9 25
FBCLK0P	143MHZ:: / 2		5 MIL SPACING		FBCLK0	::0470:0500		OUT 10
FBCLK0M	143MHZ:: / 2		5 MIL SPACING		FBCLK0	::0470:0500		OUT 10
TERM_FBCLK0P	143MHZ:: / 4		5 MIL SPACING		TERM_FBCLK0			OUT 10 11
TERM_FBCLK0M	143MHZ:: / 4		5 MIL SPACING		TERM_FBCLK0			OUT 10 11

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6101 | REV. 12

SCALE NONE | SHT 37 OF 44

CONSTRAINTS -- GRAPHICS (2 OF 2)

GRAPHICS RELATED DOO-DAHS

SIG_NAME	PULSE_PARAM / MAX_VIA_COUNT	MAX_EXPOSED_LENGTH / STUB_LENGTH	RATSNET_SCHEDULE		NET_SPACING_TYPE	DELAY_RULE	
GRAPH_XTALIN	14MHZ / 4	200 / 250			10 MIL SPACING		OUT 9
GRAPH_XTALOUT	14MHZ / 3	200 / 250			10 MIL SPACING		OUT 9
FBD<63>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<62>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<61>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<60>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<59>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<58>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<57>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<56>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<55>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<54>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<53>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<52>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<51>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<50>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<49>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<48>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<47>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<46>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<45>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<44>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<43>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<42>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<41>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<40>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<39>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<38>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<37>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<36>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<35>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<34>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<33>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<32>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<31>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<30>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<29>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<28>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<27>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<26>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<25>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<24>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<23>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<22>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<21>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<20>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<19>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<18>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<17>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<16>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<15>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<14>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<13>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<12>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<11>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<10>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<9>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<8>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<7>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<6>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<5>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<4>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<3>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<2>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<1>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<0>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBCS0*	143MHZ / 2	200 /			7.5 MIL SPACING	::0400:0700	OUT 10
TERM_FBCS0*	143MHZ / 4	200 /	FAR_END_CLUSTER		7.5 MIL SPACING		OUT 10 11
FBRAS*	143MHZ / 2	200 /			7.5 MIL SPACING	::0400:0700	OUT 10
TERM_FBRAS*	143MHZ / 4	200 /	FAR_END_CLUSTER		7.5 MIL SPACING		OUT 10 11
FBCAS*	143MHZ / 2	200 /			7.5 MIL SPACING	::0400:0700	OUT 10
TERM_FBCAS*	143MHZ / 4	200 /	FAR_END_CLUSTER		7.5 MIL SPACING		OUT 10 11
FBWE*	143MHZ / 2	200 /			7.5 MIL SPACING	::0400:0700	OUT 10
TERM_FBWE*	143MHZ / 4	200 /	FAR_END_CLUSTER		7.5 MIL SPACING		OUT 10 11
FBCKE	143MHZ / 2	200 /			7.5 MIL SPACING	::0400:0700	OUT 10
TERM_FBCKE	143MHZ / 4	200 /	FAR_END_CLUSTER		7.5 MIL SPACING		OUT 10 11
G_FBDQS1	143MHZ / 2	200 /			7.5 MIL SPACING	::0500:0600	OUT 10
TERM_FBDQS1	143MHZ / 4	200 /			7.5 MIL SPACING	::5800:6200	OUT 10 11
M_FBDQS1	143MHZ / 2	200 /			7.5 MIL SPACING	::0150:0250	OUT 11
G_FBDQS5	143MHZ / 3	200 /			7.5 MIL SPACING	::0500:0600	OUT 10
TERM_FBDQS5	143MHZ / 4	200 /			7.5 MIL SPACING	::5800:6200	OUT 10 11
M_FBDQS5	143MHZ / 2	200 /			7.5 MIL SPACING	::0150:0250	OUT 11
G_SSCLK_REFOUT	14MHZ 4	200 250			10 MIL SPACING	:::500	OUT 12
G_SSCLK_MODOUT	14MHZ 3	200 250			10 MIL SPACING	:::500	OUT 12
T_SSCLK_REFOUT	14MHZ 3	200 250			10 MIL SPACING	:::1500	OUT 9 12
GRAPH_XTALSIN	14MHZ 3	200 250			10 MIL SPACING	:::1500	OUT 9 12
G_SSCLK_XI	14MHZ 3	200 250			10 MIL SPACING	:::500	OUT 12
G_SSCLK_XO	14MHZ 3	200 250			10 MIL SPACING	:::500	OUT 12

MORE GRAPHICS RELATED DOO-DAHS

SIG_NAME	PULSE_PARAM / MAX_VIA_COUNT	RATSNET_SCHEDULE	STUB_LENGTH	NET_SPACING_TYPE	DELAY_RULE	
FBA<13>	143MHZ 2		200	7.5 MIL SPACING	::0400:0700	OUT 10
FBA<12>	143MHZ / 3		200	7.5 MIL SPACING	::0400:0700	OUT 10
FBA<11>	143MHZ / 2		200	7.5 MIL SPACING	::0400:0700	OUT 10
FBA<10>	143MHZ / 2		200	7.5 MIL SPACING	::0400:0700	OUT 10
FBA<9>	143MHZ / 2		200	7.5 MIL SPACING	::0400:0700	OUT 10
FBA<8>	143MHZ / 2		200	7.5 MIL SPACING	::0400:0700	OUT 10
FBA<7>	143MHZ / 2		200	7.5 MIL SPACING	::0400:0700	OUT 10
FBA<6>	143MHZ / 2		200	7.5 MIL SPACING	::0400:0700	OUT 10
FBA<5>	143MHZ / 2		200	7.5 MIL SPACING	::0400:0700	OUT 10
FBA<4>	143MHZ / 2		200	7.5 MIL SPACING	::0400:0700	OUT 10
FBA<3>	143MHZ / 2		200	7.5 MIL SPACING	::0400:0700	OUT 10
FBA<2>	143MHZ / 2		200	7.5 MIL SPACING	::0400:0700	OUT 10
FBA<1>	143MHZ / 2		200	7.5 MIL SPACING	::0400:0700	OUT 10
FBA<0>	143MHZ / 2		200	7.5 MIL SPACING	::0400:0700	OUT 10
TERM_FBA<13>	143MHZ 5	FAR_END_CLUSTER	200	7.5 MIL SPACING		OUT 10 11 10 11
TERM_FBA<12>	143MHZ / 5	FAR_END_CLUSTER	200	7.5 MIL SPACING		OUT 10 11
TERM_FBA<11>	143MHZ / 5	FAR_END_CLUSTER	200	7.5 MIL SPACING		OUT 10 11
TERM_FBA<10>	143MHZ / 5	FAR_END_CLUSTER	200	7.5 MIL SPACING		OUT 10 11
TERM_FBA<9>	143MHZ / 5	FAR_END_CLUSTER	200	7.5 MIL SPACING		OUT 10 11
TERM_FBA<8>	143MHZ / 5	FAR_END_CLUSTER	200	7.5 MIL SPACING		OUT 10 11
TERM_FBA<7>	143MHZ / 5	FAR_END_CLUSTER	200	7.5 MIL SPACING		OUT 10 11
TERM_FBA<6>	143MHZ / 5	FAR_END_CLUSTER	200	7.5 MIL SPACING		OUT 10 11
TERM_FBA<5>	143MHZ / 5	FAR_END_CLUSTER	200	7.5 MIL SPACING		OUT 10 11
TERM_FBA<4>	143MHZ / 5	FAR_END_CLUSTER	200	7.5 MIL SPACING		OUT 10 11
TERM_FBA<3>	143MHZ / 5	FAR_END_CLUSTER	200	7.5 MIL SPACING		OUT 10 11
TERM_FBA<2>	143MHZ / 5	FAR_END_CLUSTER	200	7.5 MIL SPACING		OUT 10 11
TERM_FBA<1>	143MHZ / 5	FAR_END_CLUSTER	200	7.5 MIL SPACING		OUT 10 11
TERM_FBA<0>	143MHZ / 5	FAR_END_CLUSTER	200	7.5 MIL SPACING		OUT 10 11
FBDQM<7>	143MHZ / 4		200	7.5 MIL SPACING	::1600:2700	OUT 10 11
FBDQM<6>	143MHZ / 4		200	7.5 MIL SPACING	::1600:2700	OUT 10 11
FBDQM<5>	143MHZ / 4		200	7.5 MIL SPACING	::1600:2700	OUT 10 11
FBDQM<4>	143MHZ / 4		200	7.5 MIL SPACING	::1600:2700	OUT 10 11
FBDQM<3>	143MHZ / 4		200	7.5 MIL SPACING	::1600:2700	OUT 10 11
FBDQM<2>	143MHZ / 4		200	7.5 MIL SPACING	::1600:2700	OUT 10 11
FBDQM<1>	143MHZ / 4		200	7.5 MIL SPACING	::1600:2700	OUT 10 11
FBDQM<0>	143MHZ / 4		200	7.5 MIL SPACING	::1600:2700	OUT 10 11
ANALOG_BLU	66MHZ / 3			15 MIL SPACING		OUT 9 25
ANALOG_GRN	66MHZ / 3			15 MIL SPACING		OUT 9 25
ANALOG_RED	66MHZ / 3			15 MIL SPACING		OUT 9 25
FILTERED_ANALOG_BLU	66MHZ / 2		20			OUT 25
FILTERED_ANALOG_GRN	66MHZ / 2		20			OUT 25
FILTERED_ANALOG_RED	66MHZ / 2		20			OUT 25

SIG_NAME	PULSE_PARAM	MAX_EXPOSED_LENGTH	ECL	DIFFERENTIAL_PAIR	MAX_VIA_COUNT	STUB_LENGTH	DELAY_RULE	NET_SPACING_TYPE
UIDE_DA<0>	66MHZ				6		::5170:6000	10 MIL SPACING
UIDE_DA<1>	66MHZ				6		::5170:5920	10 MIL SPACING
UIDE_DA<2>	66MHZ				6		::5170:6100	10 MIL SPACING
UIDE_DSTB_RDY	66MHZ				6		::5170:5920	10 MIL SPACING
UIDE_CS0_L	66MHZ				6		::5170:5920	10 MIL SPACING
UIDE_CS1_L	66MHZ				6		::5000:6700	10 MIL SPACING
UIDE_RESET_L	66MHZ				6		::1600:2000	10 MIL SPACING
UIDE_STOP	66MHZ				6		::5170:5920	10 MIL SPACING
UIDE_HSTB_RDY	66MHZ				6		::5170:5920	10 MIL SPACING
UIDE_DMAACK_L	66MHZ				6		::5170:5920	10 MIL SPACING
UIDE_DMAREQ	66MHZ				6		::5170:5920	10 MIL SPACING
UIDE_IRQ	66MHZ				6		::5170:5920	10 MIL SPACING
UIDE_D<0>	66MHZ				6		::5170:5920	10 MIL SPACING
UIDE_D<1>	66MHZ				6		::5170:5920	10 MIL SPACING
UIDE_D<2>	66MHZ				6		::5170:5920	10 MIL SPACING
UIDE_D<3>	66MHZ				6		::5170:5920	10 MIL SPACING
UIDE_D<4>	66MHZ				6		::5170:5920	10 MIL SPACING
UIDE_D<5>	66MHZ				6		::5170:5920	10 MIL SPACING
UIDE_D<6>	66MHZ				6		::5170:5920	10 MIL SPACING
UIDE_D<7>	66MHZ				6		U6.J30:RP25.4:5170:5920	10 MIL SPACING
UIDE_D<8>	66MHZ				6		::5170:5920	10 MIL SPACING
UIDE_D<9>	66MHZ				6		::5170:5920	10 MIL SPACING
UIDE_D<10>	66MHZ				6		::5000:5920	10 MIL SPACING
UIDE_D<11>	66MHZ				6		::5170:5920	10 MIL SPACING
UIDE_D<12>	66MHZ				6		::5170:5920	10 MIL SPACING
UIDE_D<13>	66MHZ				6		::5170:5920	10 MIL SPACING
UIDE_D<14>	66MHZ				6		::5130:5920	10 MIL SPACING
UIDE_D<15>	66MHZ				6		::5170:5920	10 MIL SPACING
T_UIDE_RESET_L	66MHZ				6	100	R141.2:J14.1:3508:3858	10 MIL SPACING
L1_TXCLK	2.5MHZ,25MHZ				4	100	::300:500	10 MIL SPACING
L1_RXCLK	2.5MHZ,25MHZ				4		::300:500	10 MIL SPACING
MII_TX_CLK	2.5MHZ,25MHZ				4	100	:::6000	10 MIL SPACING
MII_RX_CLK	2.5MHZ,25MHZ	250			4	100	:::6000	10 MIL SPACING
TPFOP	10MHZ,100MHZ	200			2	100		10 MIL SPACING
TPFON	10MHZ,100MHZ	202			2	100		10 MIL SPACING
TPFIP	10MHZ,100MHZ	200			2	100		10 MIL SPACING
TPFIN	10MHZ,100MHZ	225			2	100		10 MIL SPACING
TPFIP2	10MHZ,100MHZ	900			2	100		10 MIL SPACING
TPFIN2	10MHZ,100MHZ	400			2	100		10 MIL SPACING
TXP	10MHZ,100MHZ				2	100		
TXN	10MHZ,100MHZ				2	100		
RXP	10MHZ,100MHZ				2	100		
RXN	10MHZ,100MHZ				2	100		
TXCT	10MHZ,100MHZ				2	100		
RXCT	10MHZ,100MHZ				2	100		
ETH_XI	25MHZ	250			3	100	:::1500	10 MIL SPACING
ETH_XO	25MHZ	250			3	100	:::1500	10 MIL SPACING
PAN_XI	18.432MHZ				3		:::1100	10 MIL SPACING
PAN_XO	18.432MHZ	250			2	100	:::1000	10 MIL SPACING
PAN_XT	18.432MHZ				2		:::500	10 MIL SPACING
PMU_XO	10MHZ	250			2	100	:::1000	10 MIL SPACING
PMU_XI	10MHZ				2	100	:::1000	10 MIL SPACING
PMU_XT	10MHZ				2	100	:::1000	10 MIL SPACING
PMU_CLKOUT	0.032768MHZ	250			2	100	:::1000	10 MIL SPACING
PMU_CLKIN	0.032768MHZ				2	100	:::1000	10 MIL SPACING
PMU_CLKT	0.032768MHZ	250			2	100	:::1000	10 MIL SPACING

SIG_NAME	ECL
USB_DCM	TRUE
USB_DCP	TRUE
USB_DAM	TRUE
USB_DAP	TRUE
USB_DBM	TRUE
USB_DBP	TRUE
USB_DCM_F	TRUE
USB_DCP_F	TRUE
USB_DAM_F	TRUE
USB_DAP_F	TRUE
USB_DBM_F	TRUE
USB_DBP_F	TRUE
USB_DCM_EMI	TRUE
USB_DCP_EMI	TRUE
USB_DAM_EMI	TRUE
USB_DAP_EMI	TRUE
USB_DBM_EMI	TRUE
USB_DBP_EMI	TRUE

SIG_NAME	NET_SCHED
IODATA<0>	U6.P34 R138.2 R137.1 U7.25 J22.30
IODATA<1>	U6.R32 R143.2 R142.1 U7.26 J22.31
IODATA<2>	U6.T29 R150.2 R149.1 U7.27 J22.32
IODATA<3>	U6.T28 R145.2 R140.1 U7.28 J22.2
IODATA<4>	U6.R33 R156.2 R151.1 U7.32 J22.3
IODATA<5>	U6.R34 R139.2 R144.1 U7.33 J22.4
IODATA<6>	U6.U29 R165.2 R162.1 U7.34 J22.5
IODATA<7>	U6.T33 U7.35 J22.6
IOADDR<0>	U6.N28 U7.21 J22.29
IOADDR<1>	U6.J34 U7.20 J22.28
IOADDR<2>	U6.M30 U7.19 J22.27
IOADDR<3>	U6.L32 U7.18 J22.26
IOADDR<4>	U6.K34 U7.17 J22.25
IOADDR<5>	U6.L33 U7.16 J22.24
IOADDR<6>	U6.N29 U7.15 J22.23
IOADDR<7>	U6.M32 U7.14 J22.22
IOADDR<8>	U6.L34 U7.8 J22.12
IOADDR<9>	U6.P28 U7.7 J22.11
IOADDR<10>	U6.M33 U7.36 J22.8
IOADDR<11>	U6.P29 U7.6 J22.10
IOADDR<12>	U6.M34 U7.5 J22.21
IOADDR<13>	U6.P30 U7.4 J22.13
IOADDR<14>	U6.N33 U7.3 J22.14
IOADDR<15>	U6.R28 U7.2 J22.20
IOADDR<16>	U6.P32 U7.1 J22.19
IOADDR<17>	U6.N34 U7.40 J22.46
IOADDR<18>	U6.R29 U7.13 J22.47
IOADDR<19>	U6.P33 U7.37 J22.48
IOADDR<20>	U6.R30 U7.38 J22.49

SIG_NAME	NET_SCHED
CB_CE2*	U6.W28 RP10.4 J22.42
CB_CE1*	U6.W29 RP10.3 J22.7
CB_IORD*	U6.W33 RP10.1 J22.44
CB_IOWR*	U6.W34 RP10.2 J22.45
CB_IREQ*	U6.A32 R178.1 J22.16
CB_REG*	U6.B31 R136.1 J22.61
CB_RESET	U6.AE33 R168.2 J22.58
CB_WAIT*	U6.Y34 R148.1 J22.59
CSWE*	U6.V29 RP12.2 J22.15
CSOE*	U6.Y33 RP12.1 J22.9

2KV_ISO === 100MIL SPACING

CONSTRAINTS -- MISCELLANEOUS

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6101 | REV. 12

SCALE NONE | SHT 39 OF 44

SIG_NAME	PULSE_PARAM	MAX_VIA_COUNT	NET_SCHED	DELAY_RULE	STUB_LENGTH	NET_SPACING_TYPE	
VGER_L3D<0>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<1>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<2>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<3>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<4>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<5>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<6>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<7>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<8>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<9>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<10>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<11>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<12>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<13>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<14>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<15>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<16>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<17>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<18>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<19>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<20>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<21>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<22>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<23>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<24>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<25>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<26>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<27>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<28>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<29>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<30>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<31>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<32>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<33>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<34>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<35>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<36>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<37>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<38>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<39>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<40>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<41>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<42>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<43>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<44>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<45>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<46>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<47>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<48>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<49>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<50>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<51>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<52>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<53>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<54>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<55>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<56>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<57>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<58>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<59>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<60>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<61>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<62>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<63>	200MHZ	4		::1200:2500	100		OUT 4

SIG_NAME	PULSE_PARAM	MAX_VIA_COUNT	MIN_LIN_WIDTH	DELAY_RULE	STUB_LENGTH	NET_SPACING_TYPE	
VGER_L3A<0>	200MHZ	4		::2500:2800	100		OUT 4
VGER_L3A<1>	200MHZ	4		::2500:2800	100		OUT 4
VGER_L3A<2>	200MHZ	4		::2500:2800	100		OUT 4
VGER_L3A<3>	200MHZ	4		::2500:2800	100		OUT 4
VGER_L3A<4>	200MHZ	4		::2500:2800	100		OUT 4
VGER_L3A<5>	200MHZ	4		::2500:2800	100		OUT 4
VGER_L3A<6>	200MHZ	4		::2500:2800	100		OUT 4
VGER_L3A<7>	200MHZ	4		::2500:2800	100		OUT 4
VGER_L3A<8>	200MHZ	4		::2500:2800	100		OUT 4
VGER_L3A<9>	200MHZ	4		::2500:2800	100		OUT 4
VGER_L3A<10>	200MHZ	4		::2500:2800	100		OUT 4
VGER_L3A<11>	200MHZ	4		::2500:2800	100		OUT 4
VGER_L3A<12>	200MHZ	4		::2500:2800	100		OUT 4
VGER_L3A<13>	200MHZ	4		::2500:2800	100		OUT 4
VGER_L3A<14>	200MHZ	4		::2500:2800	100		OUT 4
VGER_L3A<15>	200MHZ	4		::2500:2800	100		OUT 4
VGER_L3A<16>	200MHZ	4		::2500:2800	100		OUT 4
VGER_L3A<17>	200MHZ	4		::2500:2800	100		OUT 4
VGER_L3CLK<0>	200MHZ	4		::2345:2355	100		OUT 4
VGER_L3CLK<1>	200MHZ	4		::2345:2355	100		OUT 4
VGER_L3CE*	200MHZ	4		::2500:2800	100		OUT 4
VGER_L3WE*	200MHZ	4		::2500:2800	100		OUT 4
VGER_L3ECLK<0>	200MHZ	4		::2545:2555	100		OUT 4
VGER_L3ECLK<1>	200MHZ	4		::2545:2555	100		OUT 4
VGER_L3ECLK<2>	200MHZ	4		::2545:2555	100		OUT 4
VGER_L3ECLK<3>	200MHZ	4		::2545:2555	100		OUT 4
L3_VREF<0>			10				OUT 4 20
L3_VREF<1>			10				OUT 4 20

CONSTRAINTS -- L3

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6101	12

SCALE	SHT	OF
NONE	40	44

BT1	23	BATTERY	C95	10	CAP	C190	4	CAP	C285	32	CAP	C380	32	CAP
C1	19	CAP_P	C96	29	CAP	C191	22	CAP_P	C286	16	CAP	C381	26	CAP
C2	19	CAP_P	C97	31	CAP	C192	4	CAP	C287	32	CAP	C382	26	CAP
C3	25	CAP	C98	11	CAP	C193	4	CAP	C288	15	CAP	C383	31	CAP
C4	19	CAP_P	C99	11	CAP	C194	24	CAP	C289	15	CAP	C384	26	CAP
C5	25	CAP	C100	10	CAP	C195	4	CAP	C290	16	CAP	C385	26	CAP
C6	16	CAP	C101	10	CAP	C196	4	CAP	C291	15	CAP	C386	22	CAP
C7	16	CAP	C102	10	CAP	C197	22	CAP_P	C292	9	CAP	C387	26	CAP
C8	16	CAP	C103	9	CAP	C198	24	CAP	C293	9	CAP	C388	32	CAP
C9	16	CAP	C104	9	CAP	C199	27	CAP	C294	15	CAP	C389	22	CAP
C10	25	CAP	C105	9	CAP	C200	27	CAP	C295	16	CAP	C390	32	CAP
C11	25	CAP	C106	9	CAP	C201	21	CAP_P	C296	16	CAP	C391	26	CAP
C12	16	CAP	C107	9	CAP	C202	21	CAP_P	C297	15	CAP	C392	26	CAP
C13	16	CAP	C108	10	CAP	C203	22	CAP	C298	15	CAP	C393	26	CAP
C14	16	CAP	C109	10	CAP	C204	4	CAP	C299	18	CAP	C394	31	CAP
C15	16	CAP	C110	10	CAP	C205	4	CAP	C300	15	CAP	C395	31	CAP
C16	15	CAP	C111	29	CAP	C206	22	CAP_P	C301	15	CAP	C396	31	CAP
C17	15	CAP	C112	31	CAP	C207	22	CAP_P	C302	15	CAP	C397	26	CAP
C18	16	CAP	C113	11	CAP	C208	27	CAP	C303	9	CAP	C398	26	CAP
C19	16	CAP	C114	29	CAP	C209	27	CAP	C304	9	CAP	C399	26	CAP
C20	16	CAP	C115	29	CAP	C210	27	CAP	C305	16	CAP	C400	18	CAP
C21	16	CAP	C116	29	CAP	C211	21	CAP_P	C306	15	CAP	C401	7	CAP
C22	16	CAP	C117	32	CAP_P	C212	21	CAP_P	C307	9	CAP	C402	26	CAP
C23	16	CAP	C118	22	CAP_P	C213	4	CAP_P	C308	9	CAP	C403	26	CAP
C24	16	CAP	C119	22	CAP_P	C214	27	CAP	C309	15	CAP	C404	29	CAP
C25	16	CAP	C120	22	CAP_P	C215	27	CAP	C310	15	CAP	C405	8	CAP
C26	16	CAP	C121	31	CAP	C216	27	CAP	C311	22	CAP	C406	8	CAP
C27	16	CAP	C122	31	CAP	C217	27	CAP	C312	32	CAP	C407	8	CAP
C28	16	CAP	C123	32	CAP_P	C218	27	CAP	C313	15	CAP	C408	26	CAP
C29	16	CAP_P	C124	6	CAP	C219	27	CAP	C314	15	CAP	C409	14	CAP
C30	22	CAP_P	C125	29	CAP_P	C220	22	CAP	C315	15	CAP	C410	14	CAP
C31	28	CAP_P	C126	29	CAP	C221	4	CAP	C316	22	CAP_P	C411	14	CAP
C32	25	CAP	C127	29	CAP_P	C222	4	CAP	C317	22	CAP_P	C412	14	CAP
C33	25	CAP	C128	22	CAP_P	C223	4	CAP	C318	32	CAP	C413	14	CAP
C34	16	CAP	C129	22	CAP_P	C224	22	CAP	C319	16	CAP	C414	14	CAP
C35	16	CAP_P	C130	30	CAP	C225	4	CAP	C320	16	CAP	C415	14	CAP
C36	11	CAP	C131	28	CAP	C226	4	CAP	C321	16	CAP	C416	14	CAP
C37	11	CAP	C132	29	CAP	C227	4	CAP	C322	15	CAP	C417	14	CAP
C38	11	CAP	C133	22	CAP_P	C228	4	CAP	C323	15	CAP	C418	14	CAP
C39	11	CAP	C134	28	CAP	C229	27	CAP	C324	22	CAP	C419	14	CAP
C40	11	CAP	C135	22	CAP	C230	27	CAP	C325	16	CAP	C420	14	CAP
C41	12	CAP	C136	28	CAP_P	C231	4	CAP	C326	32	CAP	C421	14	CAP
C42	11	CAP	C137	22	CAP	C232	21	CAP_P	C327	32	CAP	C422	14	CAP
C43	11	CAP	C138	26	CAP_P	C233	27	CAP	C328	11	CAP	C423	14	CAP
C44	10	CAP	C139	26	CAP	C234	22	CAP	C329	32	CAP	C424	14	CAP
C45	16	CAP	C140	26	CAP	C235	19	CAP	C330	11	CAP	C425	14	CAP
C46	10	CAP	C141	8	CAP	C236	19	CAP	C331	30	CAP	C426	14	CAP
C47	9	CAP	C142	8	CAP	C237	19	CAP	C332	11	CAP	C427	14	CAP
C48	9	CAP	C143	26	CAP	C238	19	CAP	C333	11	CAP	C428	14	CAP
C49	9	CAP	C144	26	CAP	C239	16	CAP	C334	32	CAP	C429	14	CAP
C50	9	CAP	C145	23	CAP	C240	19	CAP	C335	32	CAP	C430	14	CAP
C51	9	CAP	C146	23	CAP	C241	19	CAP	C336	6	CAP	C431	14	CAP
C52	9	CAP	C147	27	CAP	C242	32	CAP	C337	30	CAP	C432	14	CAP
C53	9	CAP	C148	28	CAP	C243	19	CAP	C338	30	CAP	C433	14	CAP
C54	9	CAP	C149	23	CAP_P	C244	19	CAP	C339	11	CAP	C434	14	CAP
C55	12	CAP	C150	23	CAP	C245	19	CAP	C340	11	CAP	C436	14	CAP
C56	30	CAP_P	C151	23	CAP	C246	16	CAP	C341	32	CAP	C437	14	CAP
C57	30	CAP_P	C152	28	CAP_P	C247	16	CAP	C342	31	CAP	C438	14	CAP
C58	10	CAP	C153	28	CAP	C248	19	CAP	C343	11	CAP	C439	14	CAP
C59	9	CAP	C154	22	CAP	C249	19	CAP	C344	29	CAP	C440	14	CAP
C60	12	CAP	C155	22	CAP_P	C250	32	CAP	C345	29	CAP	C441	14	CAP
C61	12	CAP	C156	22	CAP	C251	32	CAP	C346	29	CAP	C442	14	CAP
C62	26	CAP_P	C157	23	CAP	C252	16	CAP	C347	12	CAP	C443	14	CAP
C63	11	CAP	C158	23	CAP	C253	16	CAP	C348	11	CAP	C444	14	CAP
C64	10	CAP	C159	27	CAP_P	C254	19	CAP	C349	30	CAP	C445	14	CAP
C65	9	CAP	C160	22	CAP_P	C255	25	CAP	C350	30	CAP	C446	14	CAP
C66	9	CAP	C161	27	CAP_P	C256	25	CAP	C351	29	CAP	C447	14	CAP
C67	28	CAP	C162	27	CAP_P	C257	32	CAP	C352	11	CAP	C448	8	CAP
C68	9	CAP	C163	22	CAP	C258	15	CAP	C353	32	CAP	C449	8	CAP
C69	12	CAP	C164	6	CAP	C259	25	CAP	C354	32	CAP	C450	8	CAP
C70	9	CAP	C165	22	CAP_P	C260	32	CAP	C355	32	CAP	C451	14	CAP
C71	9	CAP	C166	23	CAP	C261	32	CAP	C356	32	CAP	C452	14	CAP
C72	9	CAP	C167	22	CAP	C262	32	CAP	C357	30	CAP	C453	14	CAP
C73	11	CAP	C168	27	CAP_P	C263	30	CAP	C358	29	CAP	C454	14	CAP
C74	9	CAP	C169	23	CAP	C264	32	CAP	C359	11	CAP	C455	14	CAP
C75	9	CAP	C170	27	CAP_P	C265	19	CAP	C360	11	CAP	C456	14	CAP
C76	31	CAP	C171	27	CAP_P	C266	19	CAP	C361	12	CAP	C457	14	CAP
C77	30	CAP	C172	27	CAP_P	C267	19	CAP	C362	28	CAP	C458	8	CAP
C78	10	CAP	C173	27	CAP_P	C268	30	CAP	C363	26	CAP	C459	14	CAP
C79	9	CAP	C174	27	CAP_P	C269	30	CAP	C364	29	CAP	C460	14	CAP
C80	12	CAP	C175	27	CAP_P	C270	19	CAP	C365	28	CAP	C461	14	CAP
C81	11	CAP	C176	27	CAP_P	C271	15	CAP	C366	11	CAP	C462	14	CAP
C82	9	CAP	C177	22	CAP	C272	15	CAP	C367	11	CAP	C463	14	CAP
C83	29	CAP_P	C178	22	CAP	C273	30	CAP	C368	26	CAP	C464	14	CAP
C84	11	CAP	C179	27	CAP_P	C274	25	CAP	C369	29	CAP	C465	14	CAP
C85	11	CAP	C180	27	CAP_P	C275	30	CAP	C370	29	CAP	C466	14	CAP
C86	9	CAP	C181	22	CAP	C276	15	CAP	C371	11	CAP	C467	14	CAP
C87	9	CAP	C182	22	CAP	C277	19	CAP	C372	26	CAP	C468	14	CAP
C88	12	CAP	C183	22	CAP	C278	19	CAP	C373	31	CAP	C469	14	CAP
C89	29	CAP	C184	22	CAP	C279	19	CAP	C374	11	CAP	C470	14	CAP
C90	9	CAP	C185	22	CAP	C280	16	CAP	C375	31	CAP	C471	14	CAP
C91	10	CAP	C186	21	CAP_P	C281	16	CAP	C376	11	CAP	C472	14	CAP
C92	9	CAP	C187	22	CAP_P	C282	15	CAP	C377	11	CAP	C473	14	CAP
C93	11	CAP	C188	4	CAP	C283	19	CAP	C378	32	CAP	C474	14	CAP
C94	10	CAP	C189	4	CAP	C284	19	CAP	C379	32	CAP	C475	14	CAP

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
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SCALE	SHT	OF
NONE	?	?

C476	14	CAP	C571	14	CAP	C667	24	CAP	D7	27	DIODE_SCHOT	L36	30	IND
C477	14	CAP	C572	14	CAP	C668	27	CAP	D8	27	DIODE_SCHOT	L37	30	IND
C478	14	CAP	C573	14	CAP	C669	27	CAP	D9	27	DIODE_SCHOT	L38	30	IND
C479	14	CAP	C574	14	CAP	C670	27	CAP	D10	32	ZENER_MMBZ15VDLT1	L39	30	IND
C480	14	CAP	C575	14	CAP	C671	24	CAP	D11	32	DIODE_SCHOT_3P	L40	30	IND
C481	14	CAP	C576	14	CAP	C672	24	CAP	D12	30	DIODE_SCHOT_3P	L41	15	IND
C482	14	CAP	C577	5	CAP	C673	24	CAP	D13	16	DIODE	L42	15	IND
C483	14	CAP	C578	14	CAP	C674	24	CAP	D14	22	DIODE_SCHOT	L43	26	IND
C484	14	CAP	C579	14	CAP	C675	24	CAP	D15	22	DIODE_SCHOT	L44	26	IND
C485	14	CAP	C580	14	CAP	C676	24	CAP	D16	22	DIODE_SCHOT	L45	25	IND
C486	14	CAP	C581	14	CAP	C677	24	CAP	D17	22	DIODE_SCHOT	L46	16	IND
C487	14	CAP	C582	18	CAP	C678	24	CAP	D18	22	DIODE_SCHOT	L47	31	IND
C488	14	CAP	C583	14	CAP	C679	27	CAP	D19	22	DIODE_SCHOT	L48	31	IND
C489	14	CAP	C584	14	CAP	C680	4	CAP	D20	27	DIODE_SCHOT	L49	31	IND
C490	14	CAP	C585	14	CAP	C681	24	CAP	D21	27	DIODE_SCHOT	L50	29	IND
C491	14	CAP	C586	5	CAP	C682	24	CAP	D22	22	DIODE_SCHOT	L51	26	IND
C492	14	CAP	C587	18	CAP	C683	4	CAP	DS1	28	LED	L52	31	IND
C493	14	CAP	C588	18	CAP	C684	4	CAP	DS2	26	LED	L53	31	IND
C494	14	CAP	C589	5	CAP	C685	24	CAP	DS3	28	LED	L54	29	IND
C495	14	CAP	C590	26	CAP	C686	27	CAP	DS4	15	LED	L55	26	IND
C496	14	CAP	C591	26	CAP	C687	27	CAP	DS5	15	LED	L56	26	IND
C497	14	CAP	C592	22	CAP	C688	24	CAP	DS6	15	LED	L57	26	IND
C498	14	CAP	C593	6	CAP	C689	4	CAP	DS7	6	LED	L58	26	IND
C499	14	CAP	C595	26	CAP	C690	4	CAP	F1	16	FUSE	L59	18	IND
C500	14	CAP	C596	26	CAP	C691	4	CAP	F2	19	FUSE	L60	26	IND
C501	14	CAP	C597	23	CAP	C692	24	CAP	F3	25	FUSE	L61	31	IND
C502	14	CAP	C598	23	CAP	C693	24	CAP	FL1	16	FILTER_CHOKE_DUAL	L62	26	IND
C503	14	CAP	C599	22	CAP	C694	4	CAP	FL2	25	FILTER_LC	L63	26	IND
C504	14	CAP	C600	27	CAP	C695	4	CAP	FL3	16	FILTER_CHOKE_DUAL	L64	26	IND
C505	14	CAP	C601	27	CAP	C696	24	CAP	FL4	25	FILTER_LC	L65	26	IND
C506	14	CAP	C602	27	CAP	C697	4	CAP	FL5	25	FILTER_LC	L66	26	IND
C507	14	CAP	C603	27	CAP	C698	4	CAP	FL6	19	FILTER_12P	L67	26	IND
C508	14	CAP	C604	27	CAP	C699	24	CAP	FL7	32	FILTER_12P	L68	7	IND
C509	14	CAP	C605	27	CAP	C700	27	CAP	J1	15	CON_RJ45	L69	7	IND
C510	14	CAP	C606	22	CAP	C701	27	CAP	J2	19	CON_F4RT_USB_UPRIGHT	Q1	30	TRA_2N3904
C511	14	CAP	C607	24	CAP	C702	27	CAP	J3	19	CON_F4RT_USB_UPRIGHT	Q2	30	TRA_2N3904
C512	14	CAP	C608	22	CAP	C703	27	CAP	J4	16	CON_FWVERT_SKT	Q3	16	TRA_2N3904
C513	14	CAP	C609	24	CAP	C704	27	CAP	J5	19	CON_F4RT_USB_UPRIGHT	Q4	30	TRA_2N3906
C514	14	CAP	C610	24	CAP	C705	4	CAP	J6	16	CON_FWVERT_SKT	Q5	30	TRA_2N7002
C515	14	CAP	C611	24	CAP	C706	24	CAP	J7	32	CON_F8RT_S_TH1	Q6	28	TRA_2N7002
C516	14	CAP	C612	24	CAP	C707	24	CAP	J8	25	CON_F14RT_D4MT_TH1	Q7	28	TRA_SI3443DV
C517	14	CAP	C613	24	CAP	C708	24	CAP	J9	30	CON_F5RT_S_2MT_TH1	Q8	28	TRA_2N7002
C518	14	CAP	C614	24	CAP	C709	21	CAP	J10	25	CON_F21RT_S2MT_SM	Q9	28	TRA_SI3443DV
C519	14	CAP	C615	22	CAP	C710	24	CAP	J11	13	CON_M4ST_LCK	Q10	28	TRA_2N7002
C520	14	CAP	C616	4	CAP	C711	24	CAP	J12	26	CON_M40SM_635	Q11	27	TRA_2N7002
C521	14	CAP	C617	3	CAP	C712	24	CAP	J13	26	CON_M26ST_SMBM	Q12	27	TRA_2N7002
C522	14	CAP	C618	24	CAP	C713	24	CAP	J14	26	CON_M40ST_NC20	Q13	28	TRA_SI3443DV
C523	14	CAP	C619	4	CAP	C714	20	CAP	J15	27	CON_M14ST_D_TH	Q14	27	TRA_2N7002
C524	22	CAP	C620	4	CAP	C715	4	CAP	J17	28	CON_M12ST_SM	Q15	28	TRA_2N7002
C525	14	CAP	C621	4	CAP	C716	4	CAP	J18	22	CON_M3ST_LCK	Q16	22	TRA_2N7002
C526	14	CAP	C622	4	CAP	C717	26	CAP	J19	6	CON_168ST_UDRM	Q17	27	TRA_2N3904
C527	14	CAP	C623	4	CAP	C718	4	CAP	J20	24	CON_F20SM_KX	Q18	23	TRA_2N3904
C528	14	CAP	C624	4	CAP	C719	4	CAP	J21	6	CON_144_33SM72	Q19	27	TRA_IRF7805
C529	14	CAP	C625	3	CAP	C720	20	CAP	J22	26	CON_68_PCMCIA_FOXCN	Q20	27	TRA_2N7002
C530	6	CAP	C626	3	CAP	C721	22	CAP	J23	24	CON_F140SM_BTB	Q21	9	TRA_2N3904
C531	6	CAP	C627	24	CAP	C722	22	CAP	J24	26	CON_M2SM_DF13	Q22	32	TRA_2N7002
C532	14	CAP	C628	24	CAP	C723	22	CAP	J25	21	CON_M6ST_BTRY	Q23	28	TRA_SI3443DV
C533	14	CAP	C629	22	CAP	C724	22	CAP_P	J26	7	CON_F1ST_S2MT_SM	Q24	32	TRA_2N7002
C534	18	CAP	C630	24	CAP	C725	7	CAP	J27	18	CON_F1ST_S2MT_SM	Q25	28	TRA_2N7002
C535	14	CAP	C631	24	CAP	C726	7	CAP	J28	3	CON_F12RT_S2MT_SM	Q26	32	TRA_2N7002
C536	14	CAP	C632	22	CAP	C727	7	CAP	L1	16	IND	Q27	28	TRA_2N7002
C537	14	CAP	C633	21	CAP	C728	7	CAP	L2	16	IND	Q28	28	TRA_2N7002
C538	14	CAP	C634	21	CAP	C729	7	CAP	L3	25	IND	Q29	27	TRA_IRF7805
C539	14	CAP	C635	24	CAP	C730	7	CAP	L4	32	IND	Q30	22	TRA_IRF7822
C540	18	CAP	C636	24	CAP	C731	7	CAP	L5	32	IND	Q31	27	TRA_IRF7805
C541	14	CAP	C637	22	CAP	C732	7	CAP	L6	9	IND	Q32	27	TRA_IRF7805
C542	14	CAP	C638	4	CAP	C733	7	CAP	L7	32	IND	Q33	22	TRA_IRF7822
C543	14	CAP	C639	4	CAP	C734	7	CAP	L8	32	IND	Q34	27	TRA_IRF7805
C544	14	CAP	C640	24	CAP	C735	7	CAP	L9	29	IND	Q35	22	TRA_IRF7822
C545	14	CAP	C641	24	CAP	C736	7	CAP	L10	29	IND	Q36	21	TRA_2N7002
C546	14	CAP	C642	4	CAP	C737	7	CAP	L11	29	IND	Q37	21	TRA_2N7002
C547	14	CAP	C643	27	CAP	C738	7	CAP	L12	32	IND	Q38	22	TRA_IRF7822
C548	14	CAP	C644	27	CAP	C739	7	CAP	L13	27	IND	R1	15	RES
C549	14	CAP	C645	24	CAP	C740	7	CAP	L14	27	IND	R2	15	RES
C550	14	CAP	C646	24	CAP	C741	7	CAP	L15	27	IND	R3	15	RES
C551	14	CAP	C647	24	CAP	C742	31	CAP	L16	13	IND	R4	15	RES
C552	14	CAP	C648	24	CAP	C743	31	CAP	L17	27	IND_3P	R5	15	RES
C553	14	CAP	C649	24	CAP	C744	31	CAP_P	L18	27	IND_3P	R6	15	RES
C554	14	CAP	C650	24	CAP	C745	21	CAP	L19	22	IND	R7	30	RES
C555	17	CAP	C651	24	CAP	C746	21	CAP	L20	32	IND	R8	15	RES
C556	14	CAP	C652	24	CAP	C748	23	CAP	L21	32	IND	R9	15	RES
C557	14	CAP	C653	24	CAP	C751	19	CAP	L22	30	IND	R10	18	RES
C558	14	CAP	C654	24	CAP	C752	22	CAP	L23	30	IND	R11	16	RES
C559	14	CAP	C655	24	CAP	C753	22	CAP	L24	30	IND	R12	16	RES
C560	14	CAP	C656	24	CAP	C754	22	CAP	L25	19	IND	R13	16	RES
C561	14	CAP	C657	24	CAP	C755	28	CAP	L26	19	IND	R14	16	RES
C562	14	CAP	C658	24	CAP	C756	28	CAP	L27	19	IND	R15	16	RES
C563	14	CAP	C659	24	CAP	C757	28	CAP	L28	19	IND	R16	15	RES
C564	14	CAP	C660	24	CAP	C758	28	CAP_P	L29	19	IND	R17	15	RES
C565	14	CAP	C661	24	CAP	D1	9	DIODE_SCHOT	L30	30	IND	R18	25	RES
C566	14	CAP	C662	24	CAP	D2	16	DIODE_SCHOT	L31	19	IND	R19	25	RES
C567	14	CAP	C663	24	CAP	D3	23	DIODE_SCHOT	L32	30	IND	R20	25	RES
C568	14	CAP	C664	24	CAP	D4	23	DIODE_SCHOT	L33	32	IND	R21	25	RES
C569	14	CAP	C665	22	CAP_P	D5	23	DIODE_SCHOT	L34	32	IND	R22	25	RES
C570	14	CAP	C666	22	CAP_P	D6	23	DIODE_SCHOT	L35	25	IND	R23	25	RES

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SIZE	DRAWING NUMBER	REV.
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NONE	?	?

R24	25	RES	R119	8	RES	R214	20	RES	R309	27	RES	R404	9	RES
R25	25	RES	R120	13	RES	R215	5	RES	R310	27	RES	R405	22	RES
R26	25	RES	R121	20	RES	R216	23	RES	R311	20	RES	R406	12	RES
R27	25	RES	R122	30	RES	R217	23	RES	R312	20	RES	R407	30	RES
R28	25	RES	R123	8	RES	R218	28	RES	R313	27	RES	R408	30	RES
R29	25	RES	R124	28	RES	R219	23	RES	R314	23	RES	R409	25	RES
R30	9	RES	R125	28	RES	R220	23	RES	R315	21	RES	R410	25	RES
R31	25	RES	R126	30	RES	R221	20	RES	R316	23	RES	R411	25	RES
R32	16	RES	R127	30	RES	R222	5	RES	R317	22	RES	R412	25	RES
R33	16	RES	R128	30	RES	R223	5	RES	R318	30	RES	R413	30	RES
R34	16	RES	R129	30	RES	R224	28	RES	R319	25	RES	R414	30	RES
R35	16	RES	R130	30	RES	R225	5	RES	R320	16	RES	R415	30	RES
R36	16	RES	R131	26	RES	R226	28	RES	R321	25	RES	R416	6	RES
R37	16	RES	R132	26	RES	R227	20	RES	R322	16	RES	R417	30	RES
R38	15	RES	R133	26	RES	R228	22	RES	R323	16	RES	R418	30	RES
R39	15	RES	R134	22	RES	R229	22	RES	R324	16	RES	R419	30	RES
R40	11	RES	R135	22	RES	R230	23	RES	R325	16	RES	R420	30	RES
R41	9	RES	R136	20	RES	R231	23	RES	R326	16	RES	R421	12	RES
R42	25	RES	R137	18	RES	R232	27	RES	R327	16	RES	R422	12	RES
R43	9	RES	R138	18	RES	R233	5	RES	R328	16	RES	R423	30	RES
R44	9	RES	R139	18	RES	R234	5	RES	R329	16	RES	R424	30	RES
R45	25	RES	R140	18	RES	R235	23	RES	R330	15	RES	R425	30	RES
R46	15	RES	R141	17	RES	R236	28	RES	R331	16	RES	R426	30	RES
R47	15	RES	R142	18	RES	R237	5	RES	R332	9	RES	R427	30	RES
R48	15	RES	R143	18	RES	R238	23	RES	R333	9	RES	R428	20	RES
R49	15	RES	R144	18	RES	R239	23	RES	R334	9	RES	R429	29	RES
R50	12	RES	R145	18	RES	R240	23	RES	R335	19	RES	R430	12	RES
R51	9	RES	R146	20	RES	R241	23	RES	R336	18	RES	R431	20	RES
R52	12	RES	R147	8	RES	R242	23	RES	R337	9	RES	R432	30	RES
R53	9	RES	R148	20	RES	R243	22	RES	R338	9	RES	R433	30	RES
R54	25	RES	R149	18	RES	R244	5	RES	R339	16	RES	R434	29	RES
R55	12	RES	R150	18	RES	R245	5	RES	R340	15	RES	R435	29	RES
R56	9	RES	R151	18	RES	R246	5	RES	R341	15	RES	R436	11	RES
R57	9	RES	R152	6	RES	R247	5	RES	R342	15	RES	R437	32	RES
R58	9	RES	R153	13	RES	R248	3	RES	R343	18	RES	R438	32	RES
R59	16	RES	R154	8	RES	R249	3	RES	R344	18	RES	R439	29	RES
R60	16	RES	R155	18	RES	R250	3	RES	R345	32	RES	R440	28	RES
R61	9	RES	R156	18	RES	R251	3	RES	R346	9	RES	R441	28	RES
R62	28	RES	R157	26	RES	R252	3	RES	R347	9	RES	R442	29	RES
R63	25	RES	R158	6	RES	R253	23	RES	R348	25	RES	R443	31	RES
R64	20	RES	R159	13	RES	R254	23	RES	R349	25	RES	R444	29	RES
R65	25	RES	R160	6	RES	R255	28	RES	R350	25	RES	R445	12	RES
R66	20	RES	R161	18	RES	R256	5	RES	R351	25	RES	R446	12	RES
R67	10	RES	R162	18	RES	R257	23	RES	R352	25	RES	R447	31	RES
R68	31	RES	R163	18	RES	R258	22	RES	R353	25	RES	R448	29	RES
R69	31	RES	R164	6	RES	R259	20	RES	R354	25	RES	R449	28	RES
R70	31	RES	R165	18	RES	R260	20	RES	R355	15	RES	R450	31	RES
R71	31	RES	R166	20	RES	R261	20	RES	R356	15	RES	R451	29	RES
R72	30	RES	R167	18	RES	R262	22	RES	R357	15	RES	R452	12	RES
R73	16	RES	R168	18	RES	R263	3	RES	R358	32	RES	R453	12	RES
R74	30	RES	R169	13	RES	R264	3	RES	R359	15	RES	R454	32	RES
R75	30	RES	R170	18	RES	R265	3	RES	R360	22	RES	R455	32	RES
R76	10	RES	R171	18	RES	R266	3	RES	R361	22	RES	R456	31	RES
R77	10	RES	R172	18	RES	R267	3	RES	R362	32	RES	R457	11	RES
R78	9	RES	R173	18	RES	R268	23	RES	R363	15	RES	R458	11	RES
R79	20	RES	R174	5	RES	R269	22	RES	R364	25	RES	R459	20	RES
R80	11	RES	R175	18	RES	R270	28	RES	R365	25	RES	R460	22	RES
R81	11	RES	R176	23	RES	R271	22	RES	R366	25	RES	R461	22	RES
R82	20	RES	R177	23	RES	R272	22	RES	R367	25	RES	R462	32	RES
R83	20	RES	R178	20	RES	R273	22	RES	R368	25	RES	R463	32	RES
R84	28	RES	R179	20	RES	R274	20	RES	R369	25	RES	R464	20	RES
R85	31	RES	R180	20	RES	R275	20	RES	R370	9	RES	R465	32	RES
R86	11	RES	R181	18	RES	R276	20	RES	R371	9	RES	R466	32	RES
R87	20	RES	R182	5	RES	R277	20	RES	R372	16	RES	R467	10	RES
R88	10	RES	R183	18	RES	R278	27	RES	R373	15	RES	R468	10	RES
R89	20	RES	R184	27	RES	R279	22	RES	R374	22	RES	R469	10	RES
R90	31	RES	R185	23	RES	R280	20	RES	R375	32	RES	R470	10	RES
R91	10	RES	R186	23	RES	R281	20	RES	R376	32	RES	R471	10	RES
R92	20	RES	R187	28	RES	R282	20	RES	R377	16	RES	R472	10	RES
R93	9	RES	R188	28	RES	R283	20	RES	R378	16	RES	R473	10	RES
R94	20	RES	R189	5	RES	R284	20	RES	R379	16	RES	R474	29	RES
R95	9	RES	R190	28	RES	R285	20	RES	R380	16	RES	R475	26	RES
R96	32	RES	R191	28	RES	R286	20	RES	R381	16	RES	R476	26	RES
R97	10	RES	R192	5	RES	R287	20	RES	R382	11	RES	R477	26	RES
R98	10	RES	R193	18	RES	R288	20	RES	R383	11	RES	R478	26	RES
R99	10	RES	R194	18	RES	R289	20	RES	R384	20	RES	R479	29	RES
R100	10	RES	R195	23	RES	R290	20	RES	R385	20	RES	R480	31	RES
R101	10	RES	R196	23	RES	R291	20	RES	R386	9	RES	R481	31	RES
R102	10	RES	R197	23	RES	R292	20	RES	R387	11	RES	R482	31	RES
R103	10	RES	R198	23	RES	R293	20	RES	R388	11	RES	R483	26	RES
R104	10	RES	R199	23	RES	R294	20	RES	R389	11	RES	R484	22	RES
R105	10	RES	R200	23	RES	R295	20	RES	R390	32	RES	R485	19	RES
R106	10	RES	R201	23	RES	R296	20	RES	R391	30	RES	R486	6	RES
R107	31	RES	R202	23	RES	R297	27	RES	R392	30	RES	R487	19	RES
R108	31	RES	R203	23	RES	R298	27	RES	R393	30	RES	R488	29	RES
R109	31	RES	R204	23	RES	R299	27	RES	R394	30	RES	R489	29	RES
R110	29	RES	R205	23	RES	R300	27	RES	R395	25	RES	R490	19	RES
R111	29	RES	R206	23	RES	R301	27	RES	R396	15	RES	R491	19	RES
R112	29	RES	R207	23	RES	R302	27	RES	R397	12	RES	R492	19	RES
R113	29	RES	R208	23	RES	R303	27	RES	R398	15	RES	R493	19	RES
R114	8	RES	R209	27	RES	R304	22	RES	R399	15	RES	R495	19	RES
R115	8	RES	R210	23	RES	R305	24	RES	R400	15	RES	R496	18	RES
R116	8	RES	R211	23	RES	R306	20	RES	R401	15	RES	R497	20	RES
R117	8	RES	R212	23	RES	R307	21	RES	R402	12	RES	R498	8	RES
R118	8	RES	R213	23	RES	R308	27	RES	R403	25	RES	R499	8	RES

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	?	?
SCALE	SHT	OF
NONE	?	?

R500	31	RES	R595	23	RES	R746	21	RES	U31	27	LTC1628
R501	31	RES	R596	28	RES	R747	21	RES	U32	21	VREG_LP2951
R502	31	RES	R597	23	RES	R748	24	RES	U33	7	CLK_GEN_IMIC5003
R503	19	RES	R598	23	RES	R749	21	RES	U35	21	AT90S1200
R504	19	RES	R599	22	RES	R750	21	RES	U36	21	EEPR_256X8
R505	19	RES	R600	22	RES	R751	21	RES	U38	19	SWI_TPS2023
R506	13	RES	R601	28	RES	R752	21	RES	VR1	22	VREG_EZ1582
R507	19	RES	R602	20	RES	R753	21	RES	VR2	22	VREG_EZ1582
R508	19	RES	R603	20	RES	R754	21	RES	VR3	22	VREG_EZ1582
R509	13	RES	R604	20	RES	R755	32	RES	VR4	21	VREG_EZ1582
R510	31	RES	R605	27	RES	R756	32	RES	VR5	28	VREG_EZ1582
R511	13	RES	R606	27	RES	R757	20	RES	XS1	31	STAR
R512	18	RES	R607	27	RES	R760	22	RES	XS2	30	STAR
R513	13	RES	R608	20	RES	R761	7	RES	XS3	29	STAR
R514	8	RES	R609	3	RES	R762	7	RES	XS4	32	STAR
R515	8	RES	R610	27	RES	R763	7	RES	XS5	29	STAR
R516	8	RES	R611	3	RES	R764	18	RES	XW1	28	SHORT
R517	8	RES	R612	22	RES	R765	18	RES	XW2	28	SHORT
R518	8	RES	R613	22	RES	R766	18	RES	XW3	31	SHORT
R519	24	RES	R614	21	RES	R767	22	RES	XW4	22	SHORT
R520	24	RES	R615	20	RES	R768	22	RES	XW5	27	SHORT
R521	26	RES	R616	20	RES	R769	22	RES	Y1	16	CRYSTAL
R522	8	RES	R617	22	RES	R780	28	RES	Y2	15	CRYSTAL
R523	8	RES	R618	21	RES	R781	28	RES	Y3	9	CRYSTAL
R524	24	RES	R619	20	RES	RP1	20	RPAK4P	Y4	23	CRYSTAL
R525	24	RES	R620	21	RES	RP2	10	RPAK4P	Y5	23	CRYSTAL_4PIN
R526	26	RES	R621	21	RES	RP3	20	RPAK4P	Y6	18	CRYSTAL
R527	17	RES	R622	20	RES	RP4	13	RPAK4P	Y7	12	CRYSTAL
R528	24	RES	R623	20	RES	RP5	20	RPAK4P	Y8	7	CRYSTAL
R529	24	RES	R624	7	RES	RP6	13	RPAK4P	ZH1	33	MTGHOLE
R530	8	RES	R625	7	RES	RP7	6	RPAK4P	ZH2	33	MTGHOLE
R531	6	RES	R626	20	RES	RP8	20	RPAK4P	ZH3	33	MTGHOLE
R532	7	RES	R627	7	RES	RP9	8	RPAK4P	ZH4	28	MTGHOLE
R533	24	RES	R628	7	RES	RP10	20	RPAK4P	ZH40	26	PCB_STANDOFF
R534	24	RES	R629	20	RES	RP11	6	RPAK4P	ZH44	26	PCB_STANDOFF
R535	13	RES	R630	20	RES	RP12	20	RPAK4P			
R536	13	RES	R631	27	RES	RP13	20	RPAK4P			
R537	13	RES	R632	20	RES	RP14	20	RPAK4P			
R538	8	RES	R633	22	RES	RP15	20	RPAK4P			
R539	6	RES	R634	20	RES	RP16	20	RPAK4P			
R540	8	RES	R635	7	RES	RP17	20	RPAK4P			
R541	7	RES	R636	7	RES	RP18	20	RPAK4P			
R542	18	RES	R637	7	RES	RP19	15	RPAK4P			
R543	7	RES	R638	7	RES	RP20	10	RPAK4P			
R544	18	RES	R639	27	RES	RP21	8	RPAK4P			
R545	26	RES	R640	27	RES	RP22	6,8	RPAK4P			
R546	6	RES	R641	21	RES	RP23	6,8	RPAK4P			
R547	7	RES	R642	21	RES	RP24	8	RPAK4P			
R548	7	RES	R643	22	RES	RP25	17	RPAK4P			
R549	17	RES	R644	27	RES	RP26	8	RPAK4P			
R550	7	RES	R645	15	RES	RP27	17	RPAK4P			
R551	17	RES	R646	24	RES	RP28	6	RPAK4P			
R552	7	RES	R647	27	RES	RP29	6,8	RPAK4P			
R553	17	RES	R648	27	RES	RP30	17	RPAK4P			
R554	18	RES	R649	27	RES	RP31	6,8	RPAK4P			
R555	26	RES	R650	27	RES	RP32	17	RPAK4P			
R556	7	RES	R651	27	RES	RP33	8	RPAK4P			
R557	17	RES	R652	7	RES	RP34	6	RPAK4P			
R558	7	RES	R653	7	RES	RP35	7	RPAK4P			
R559	26	RES	R654	7	RES	S1	28	SWI_4RTSA1_SMB			
R560	7	RES	R655	20	RES	S2	28	SWI_4RTSA1_SMB			
R561	17	RES	R656	7	RES	S3	26	SWI_4RTSA1_SMB			
R562	5	RES	R657	7	RES	S4	23	SWI_TACT_4SM			
R563	17	RES	R667	7	RES	S5	23	SWI_TACT			
R564	5	RES	R668	7	RES	T1	15	XFR_100BT_MDIX			
R565	5	RES	R670	7	RES	U1	9	VREG_TL431			
R566	5	RES	R676	7	RES	U2	15	TRANSCEIVER_ENET_LXT971A			
R567	26	RES	R678	7	RES	U3	11	SGRAM_2MX32			
R568	18	RES	R680	7	RES	U4	32	AMP_TA2024			
R569	18	RES	R681	7	RES	U5	29	TAS3001C			
R570	5	RES	R721	20	RES	U6	5,6,8,13	PANGEA			
R571	17	RES	R722	22	RES	U7	8	FEPR_1MX8			
R572	7	RES	R723	31	RES	U8	23	M16C62			
R573	26	RES	R724	31	RES	U9	7	74574			
R574	26	RES	R725	31	RES	U10	22	VREG_LP2951			
R575	20	RES	R726	31	RES	U11	23	VREG_TL431			
R576	20	RES	R727	16	RES	U12	23	VDET_MC33465N_22ATR			
R577	20	RES	R728	4	RES	U13	3,4	SCVGER483			
R578	5	RES	R729	4	RES	U14	4	SRAM_DDR_153PBGA			
R579	5	RES	R730	4	RES	U15	23	NC7SZ04			
R580	7	RES	R731	4	RES	U16	18,25	74125			
R581	17	RES	R732	21	RES	U17	16	FW802			
R582	17	RES	R733	21	RES	U18	16	VREG_LP2951			
R583	22	RES	R734	21	RES	U19	12	CLK_GEN_IMISM530			
R584	17	RES	R735	21	RES	U20	29,30	OPAMP_TS924			
R585	17	RES	R736	21	RES	U21	11	SGRAM_2MX32			
R586	17	RES	R737	21	RES	U22	9,10,12	MONICA			
R587	23	RES	R738	21	RES	U23	29	ADDAC_TLC320AD77C			
R588	23	RES	R739	21	RES	U24	31	OPAMP_TS924			
R589	23	RES	R740	21	RES	U25	29	VREG_LP2951			
R590	28	RES	R741	21	RES	U26	29	VREG_LP2951			
R591	23	RES	R742	21	RES	U27	31	ADC_CS5331			
R592	22	RES	R743	21	RES	U28	23	MAX6328			
R593	26	RES	R744	21	RES	U29	22	SWREG_LTC1735			
R594	28	RES	R745	21	RES	U30	4	SRAM_DDR_153PBGA			

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	?	?
SCALE	SHT	OF
NONE	?	?