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- 1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
- 2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
- 3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

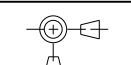
IMAC 5,2 -- REV D

10/6/06

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD	ENG APPD
E		544174	PRODUCTION RELEASED		
				DATE	DATE
				11/06/07	06/22/04

PDF	CSA	CONTENTS	SYNC	MASTER	DATE
2	2	System Block Diagram	MASTER	MASTER	
3	3	Power Block Diagram	MASTER	MASTER	
4	4	Table Items	MASTER	MASTER	
5	5	FUNC TEST 1 OF 2	MASTER	MASTER	
6	6	Power Conn / Alias	MASTER	MASTER	
7	7	CPU 1 OF 2-FSB	MASTER	MASTER	
8	8	CPU 2 OF 2-PWR/GND	MASTER	MASTER	
9	9	CPU DECAPS & VID<>	MASTER	MASTER	
10	10	CPU TEMP SENSOR	MASTER	MASTER	
11	11	CPU ITP700FLEX DEBUG	M38	01/05/2006	
12	12	NB CPU Interface	M1	01/05/2006	
13	13	NB PEG / Video Interfaces	M1	01/05/2006	
14	14	NB Misc Interfaces	MASTER	MASTER	
15	15	NB DDR2 Interfaces	M1	01/05/2006	
16	16	NB Power 1	MASTER	MASTER	
17	17	NB Power 2	M40	01/05/2006	
18	18	NB Grounds	M1	01/05/2006	
19	19	NB (GM) Decoupling	(MASTER)	(MASTER)	
20	20	NB Config Straps	M1	01/05/2006	
21	21	SB: 1 OF 4	M38	01/05/2006	
22	22	SB: 2 OF 4	MASTER	MASTER	
23	23	SB: 3 OF 4	MASTER	MASTER	
24	24	SB: 4 OF 4	M38	01/05/2006	
25	25	SB: DECOUPLING	MASTER	MASTER	
26	26	SB: MISC	MASTER	MASTER	
27	27	SB: SMB HUB AND ALIAS	MASTER	MASTER	
28	28	DDR2 SO-DIMM Connector A	MASTER	MASTER	
29	29	DDR2 SO-DIMM Connector B	MASTER	MASTER	
30	30	Memory Active Termination	MASTER	MASTER	
31	31	Memory Vtt Supply	MASTER	MASTER	
32	33	CLOCKS	MASTER	MASTER	
33	34	CLOCKS: TERMINATIONS	MASTER	MASTER	
34	38	Disk Connectors	MASTER	MASTER	
35	41	ETHERNET CONTROLLER	MASTER	MASTER	
36	42	ETHERNET MISC	MASTER	MASTER	
37	43	ETHERNET CONNECTOR	MASTER	MASTER	

PDF	CSA	CONTENTS	SYNC	MASTER	DATE
38	44	FW: FW323-06	MASTER	MASTER	
39	45	FW: DECAPS	MASTER	MASTER	
40	46	FIREWIRE CONNECTORS	MASTER	MASTER	
41	47	USB Device Interfaces	MASTER	MASTER	
42	53	AIRPORT CONN	MASTER	MASTER	
43	54	PCIE PORT ALIASES	MASTER	MASTER	
44	58	SMC	M1	01/05/2006	
45	59	SMC & TPM SUPPORT	(MASTER)	(MASTER)	
46	60	LPC+ CONN	M38	12/09/2005	
47	61	NB THERMAL	MASTER	MASTER	
48	63	SPI BOOTROM	M38	01/05/2006	
49	65	Fan 0, 1 & System Temp	MASTER	MASTER	
50	66	Fan 2 & HD Temp	MASTER	MASTER	
51	67	TPM	M38	01/05/2006	
52	68	AUDIO: CODEC	AUDIO	05/12/2006	
53	72	AUDIO: SPEAKER AMP	AUDIO	05/12/2006	
54	73	AUDIO: CONNECTORS	AUDIO	05/12/2006	
55	74	AUDIO: POWER SUPPLIES	AUDIO	05/12/2006	
56	75	IMVP6 CPU VCore Regulator	MASTER	MASTER	
57	76	CPU & SYSTEM SENSE CIRCUI	(MASTER)	(MASTER)	
58	77	PWR GOOD	(MASTER)	(MASTER)	
59	78	3V DC/DC 2.5V	(MASTER)	(MASTER)	
60	79	1.8V & 1.2V VREG	MASTER	MASTER	
61	80	1.5V_S0 & 1.05V_S0 VREG	MASTER	MASTER	
62	82	5V DC/DC	MASTER	MASTER	
63	83	S0 AND S3 FETS	MASTER	MASTER	
64	94	Internal Display Conns	MASTER	MASTER	
65	95	EXTERNAL TMDS	MASTER	MASTER	
66	96	TMDS/Inverter/ExtVGA	MASTER	MASTER	
67	97	External Display Conns	MASTER	MASTER	

DIMENSIONS ARE IN MILLIMETERS		METRIC		Apple Computer Inc.	
XX :	_____	DRAPTER	/	DESIGN CK	/
X.XX :	_____	ENG APPD	/	MFG APPD	/
X.XXX :	_____	QA APPD	/	DESIGNER	/
ANGLES :	_____	RELEASE	/	SCALE	NONE
DO NOT SCALE DRAWING		MATERIAL/FINISH NOTED AS APPLICABLE		SIZE	D
 THIRD ANGLE PROJECTION		DRAWING NUMBER		051-7199	REV. E
				SHT 1 OF 97	

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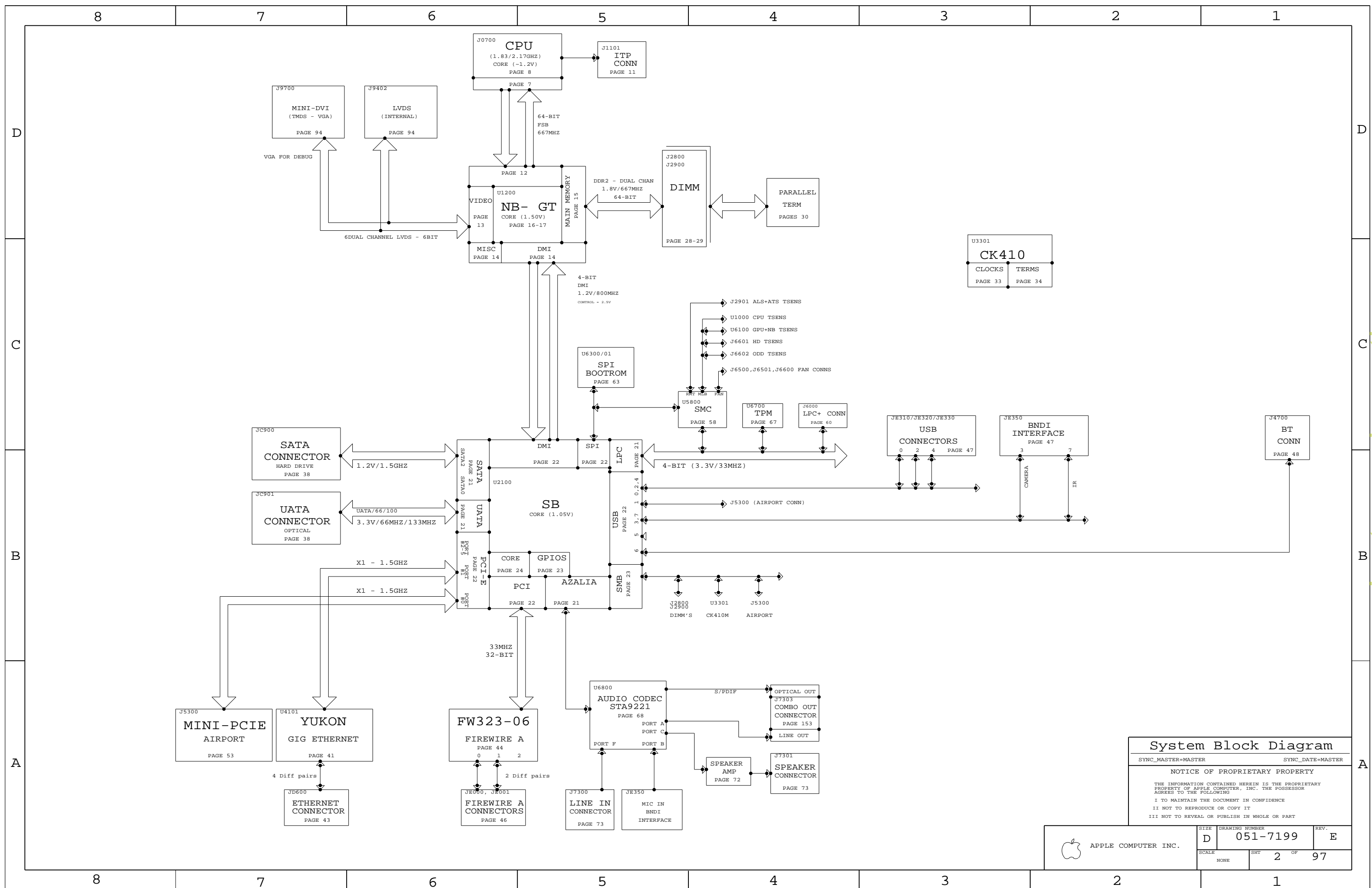
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System Block Diagram

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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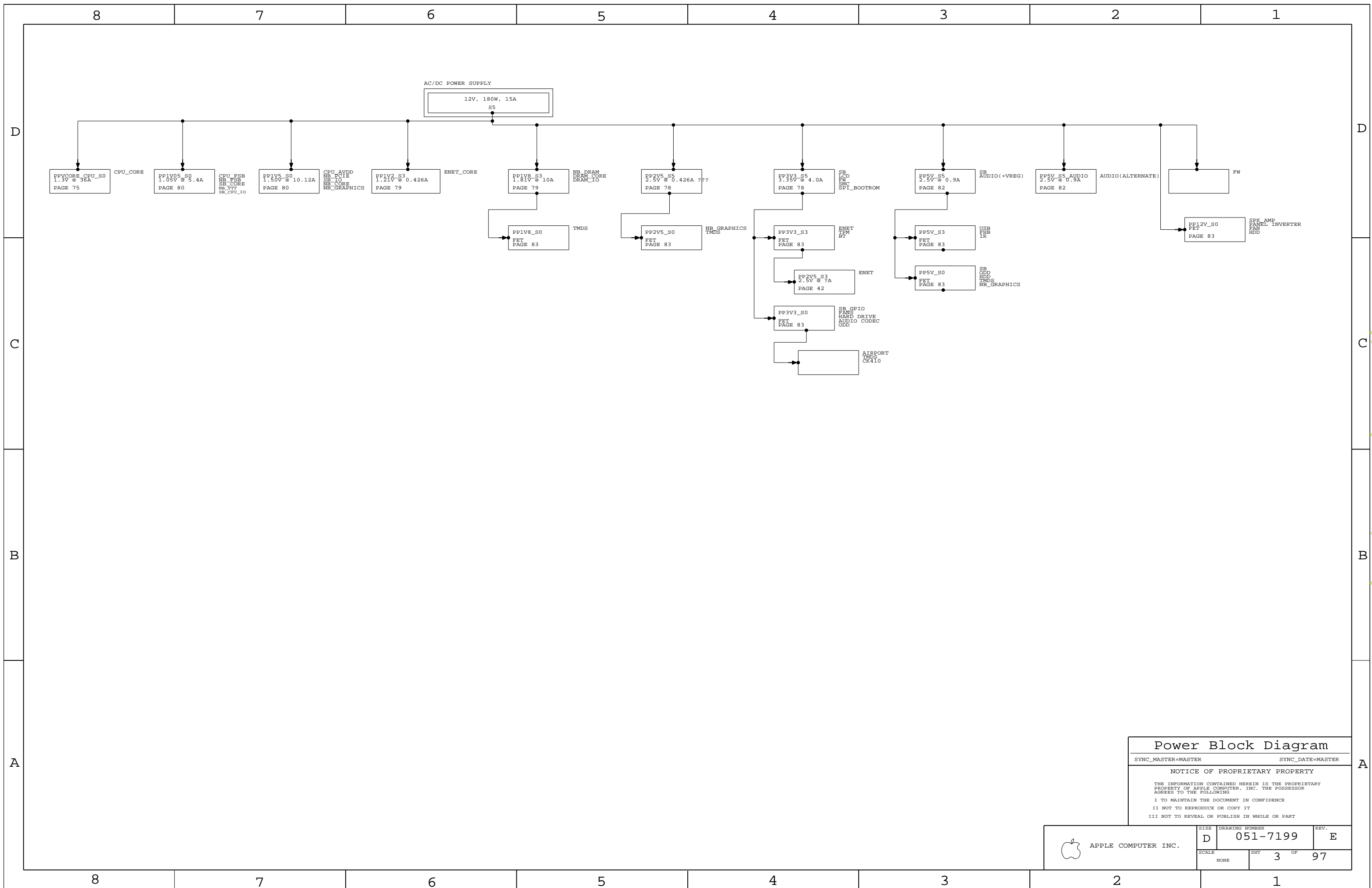
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	SCALE NONE	SHEET 2	OF 97



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Power Block Diagram
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	D	051-7199	E
SCALE	SHT	OF	REV.
NONE	3	97	

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COMMON

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
511S0025	1	IC,CPU-SKT,479BGA	J0700	CRITICAL	
338S0298	1	IC,945GT,NORTHBRIDGE	U1200	CRITICAL	
343S0385	1	IC,SB,652BGA	U2100	CRITICAL	
742-0048	1	BAT,COIN,3V,220MAH,CR2032	BT2600	CRITICAL	
359S0101	1	IC,CY28445-5,CLK GEN,68PIN QFP	U3301	CRITICAL	
338S0270	1	IC,88E8053,GIGABIT ENET XCVR,64P QFN MD	U4101	CRITICAL	
(335S0382) 341S1797	1	IC,ENET LAN ROM	U4102	CRITICAL	
338S0279	1	IC,FW32306,1394A LINK,TQFP	U4400	CRITICAL	
338S0274 341T0022	1	IC,SMC,M50	U5800	CRITICAL	
341S1789	1	IC,TPM,TSSOP,28P	U6700	CRITICAL	TPM
353S1461	1	IC,CPU VREG,IMVP,TWO PHASE	U7500	CRITICAL	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
051-7199	1	PCB,SCHM,MLB,M50	SCH1		
820-1960	1	PCB,FAB,MLB,M50	MLB1		
(335S0384) 341T0042	1	EFI ROM,M50A	U6301	CRITICAL	
337S3386	1	M50 MEROM CPU	CPU	CRITICAL	MEROM

341S1859 IC EFI BOOTROM DEV M50
 337S3242 M38 CPU(C0)
 337S3280 M50 1.83G LOW SPEED CPU (D0)
 USE BOM OPTION MEROM FOR MEROM PROCESSOR

OPS REQUESTED QUAL PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
155S0295	1	CHOKE,COMMON_MODE,1650HM,4PIN	L9703	CRITICAL	
124-0359	3	PCAP,120UF,16V,20%,ELEC	C6505,C6504,C6602	CRITICAL	

ALTERNATE PARTS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
126S0091	126S0092		C625	FACTORY SHORTAGE
353S1278	353S1381		U5940	SMC VREF
378S0141	378S0140		LX2601,LX2602,LX2603	
353S1465	353S1461		U7500	CPU VREG, OLD DIE, SCREENED PART
124-0338	124-0333		C7953,C7954	FOR SUPPLY
124-0361	124-0339		C7577,C7578,C7579,C7956,C7957	SANYO CAP
138S0598	138S0512		C624,C7201,C7203,C7232,C7811,C911,C8000,C8001,C8002,C8003,C8211,C9420	FOR SUPPLY
155S0321	155S0164		L9700,L9701,L9702	FOR SUPPLY
353S1975	353S1458		U6800	COST REDUCTION

MECHANICAL PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
603-9187	1	SUBASSY, M50 NB HEATSINK	HS2	CRITICAL	
603-9186	1	SUBASSY, M50 CPU HEATSINK	HS1	CRITICAL	
725-0668	1	MYLAR WASHER	WASH1	CRITICAL	
725-0720	1	MYLAR BLACK LED CVR, M50	CVR1	CRITICAL	
825-6447	1	BARCODE LABEL, M50A	[EEE:WZE]	CRITICAL	MEROM

Table Items

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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	D	051-7199	E
SCALE	SHT	OF	
NONE	4	97	

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LAYOUT NOTE: PLACE NEAR J0700

LAYOUT NOTE: PLACE NEAR U1200

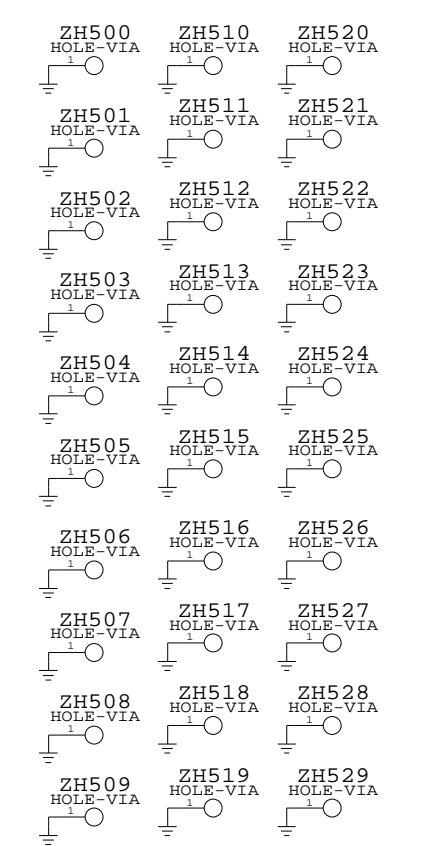
LAYOUT NOTE: PLACE NEAR U4101

PLACE NEAR R1210 AND R1211

PLACE NEAR R0705 AND R0706

PLACE NEAR R2800 AND R2801

MISC GROUND VIAS

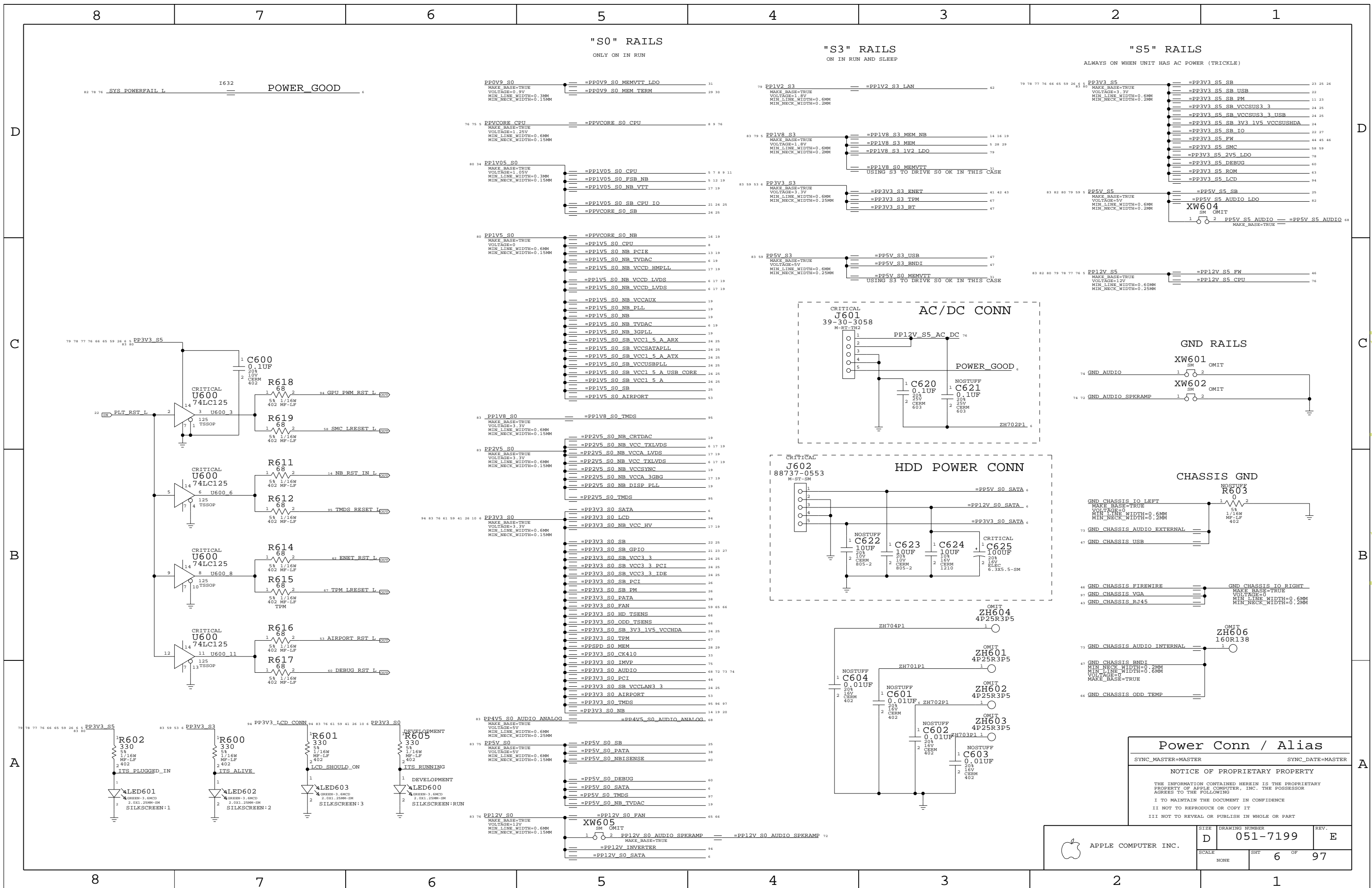


THIS TEST POINT USED TO CONNECT THE SHAPES AROUND SLOT ON TOP AND BOTTOM OF THE BOARD.

FUNC TEST 1 OF 2
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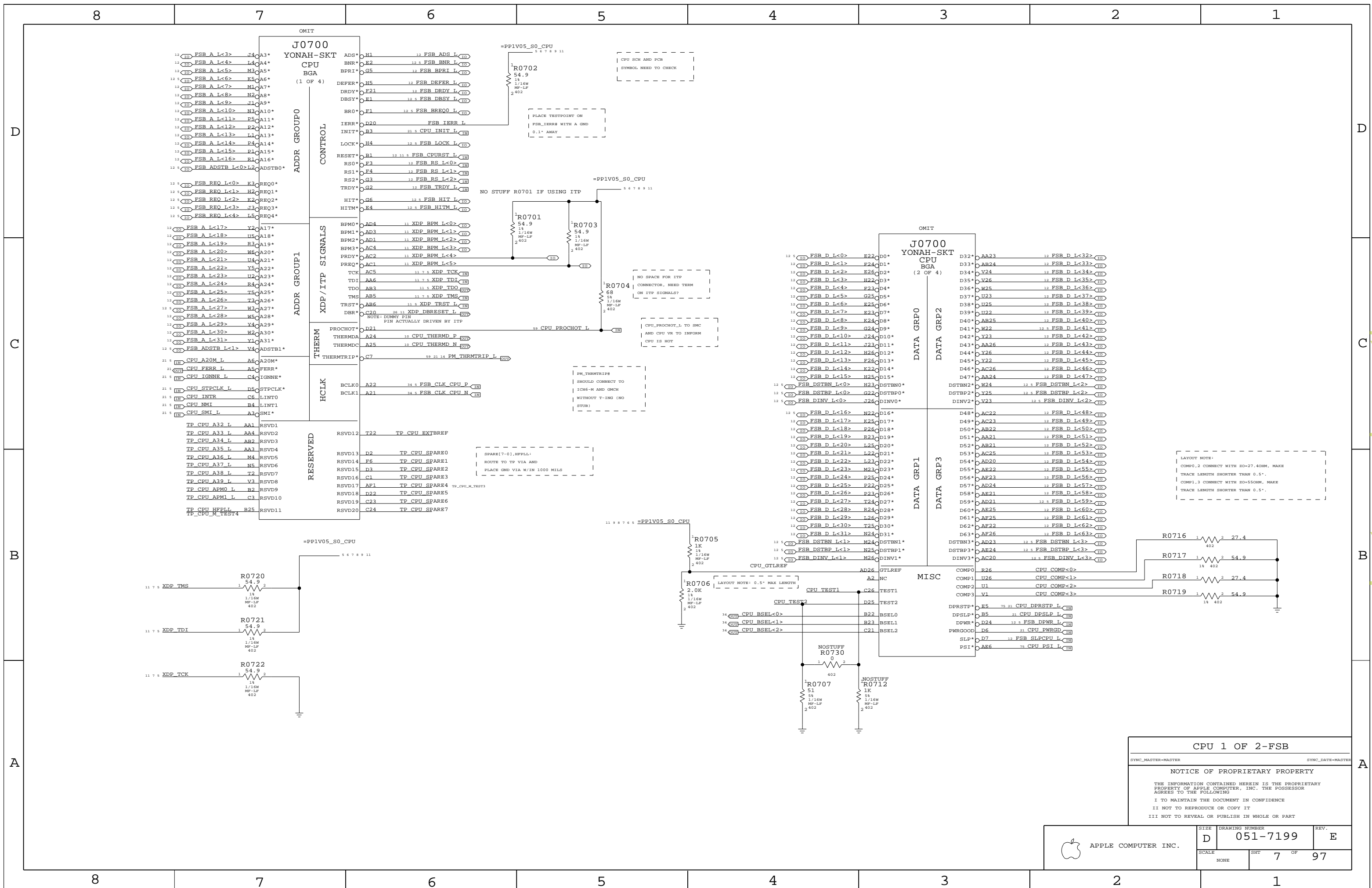
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Power Conn / Alias
 SYNC_MASTER=MASTER SYNC_DATE=MASTER
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CPU 1 OF 2-FSB

SYNC_MASTER-MASTER SYNC_DATE-MASTER

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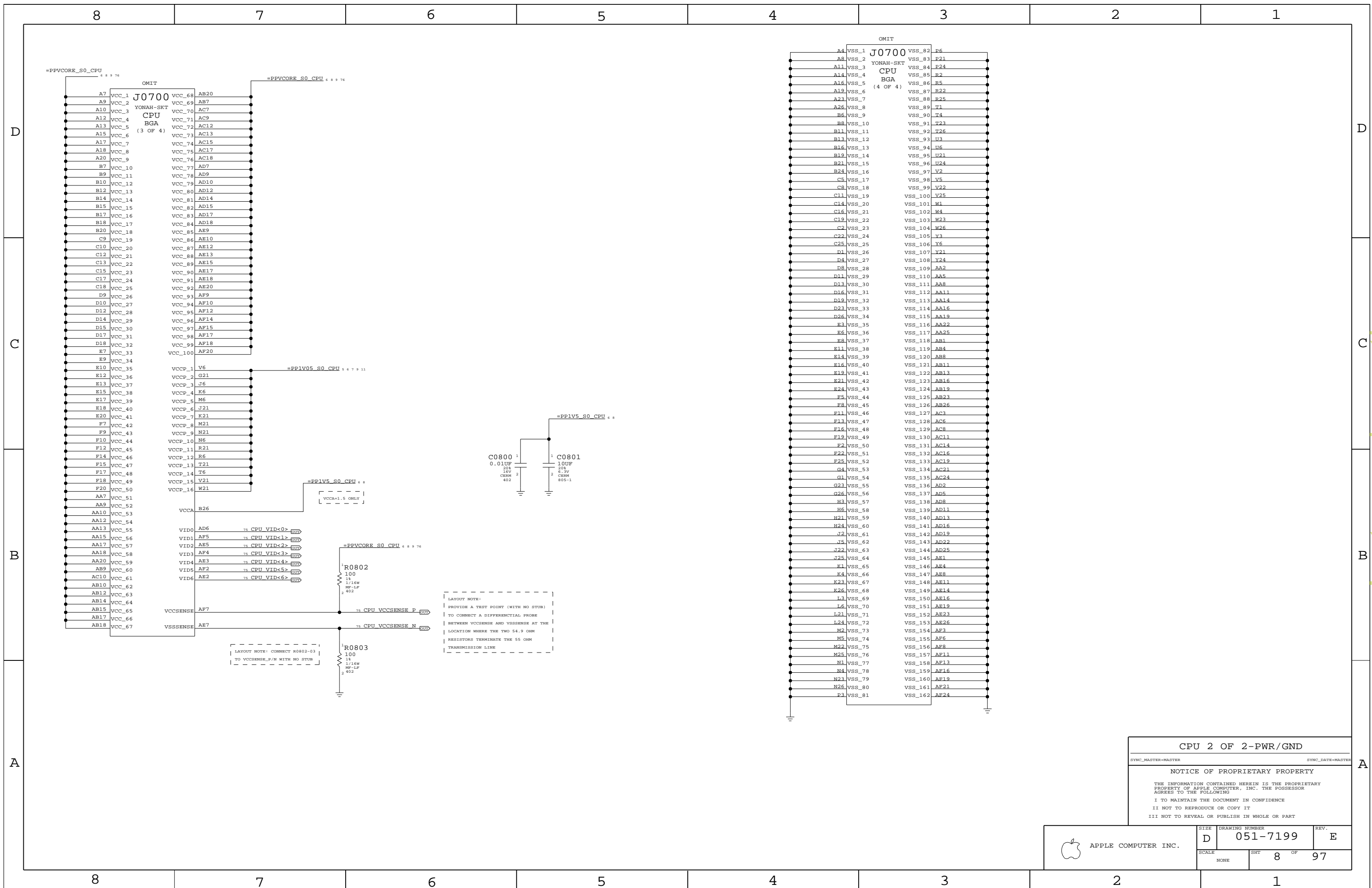
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	SCALE NONE	SHEET 7 OF 97	



CPU 2 OF 2-PWR/GND

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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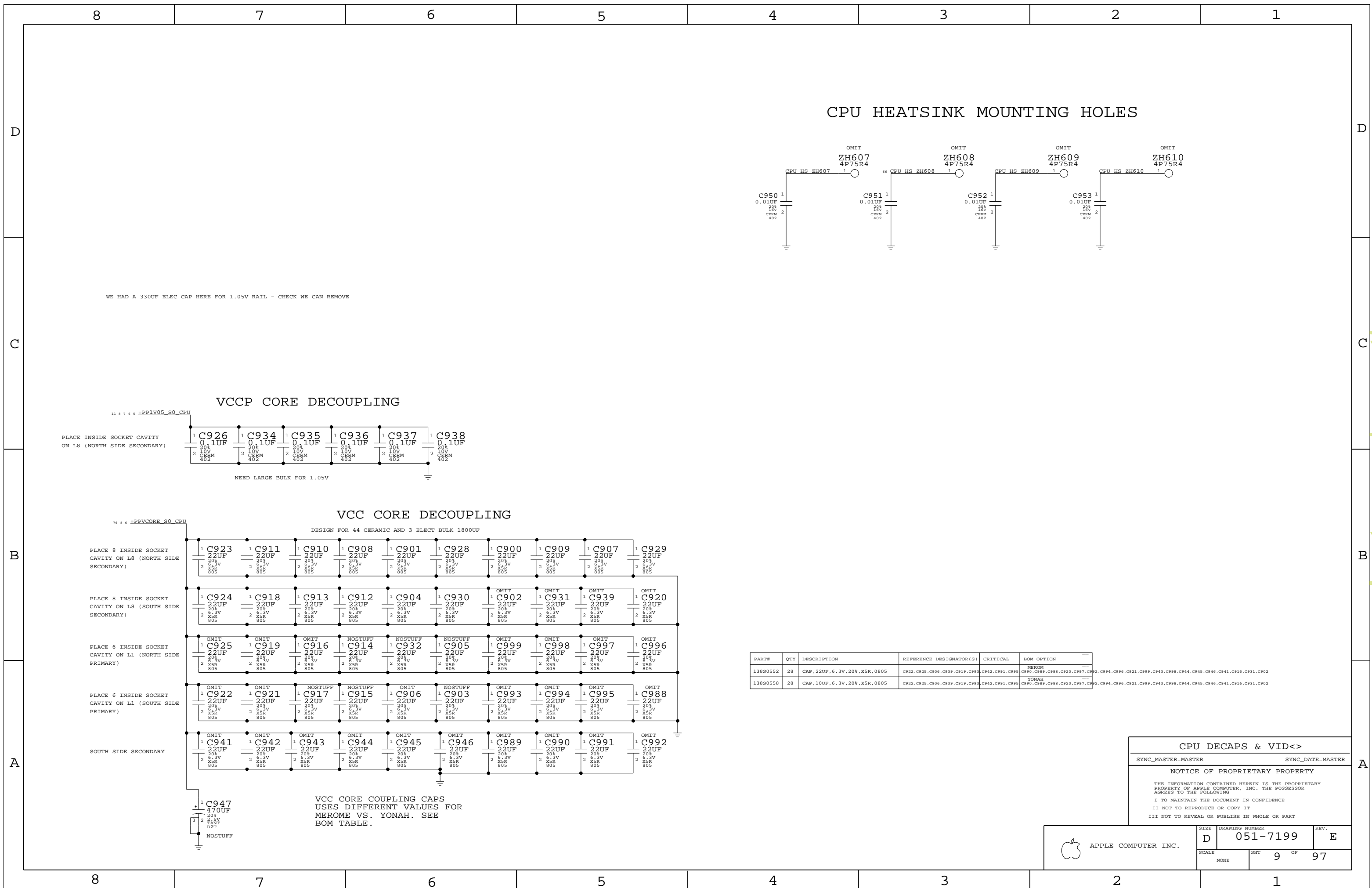
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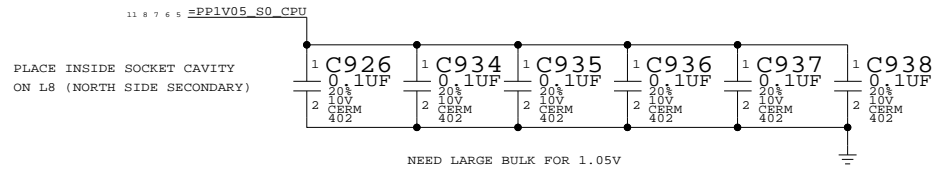
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SCALE	SHT	OF	REV.
NONE	8	97	

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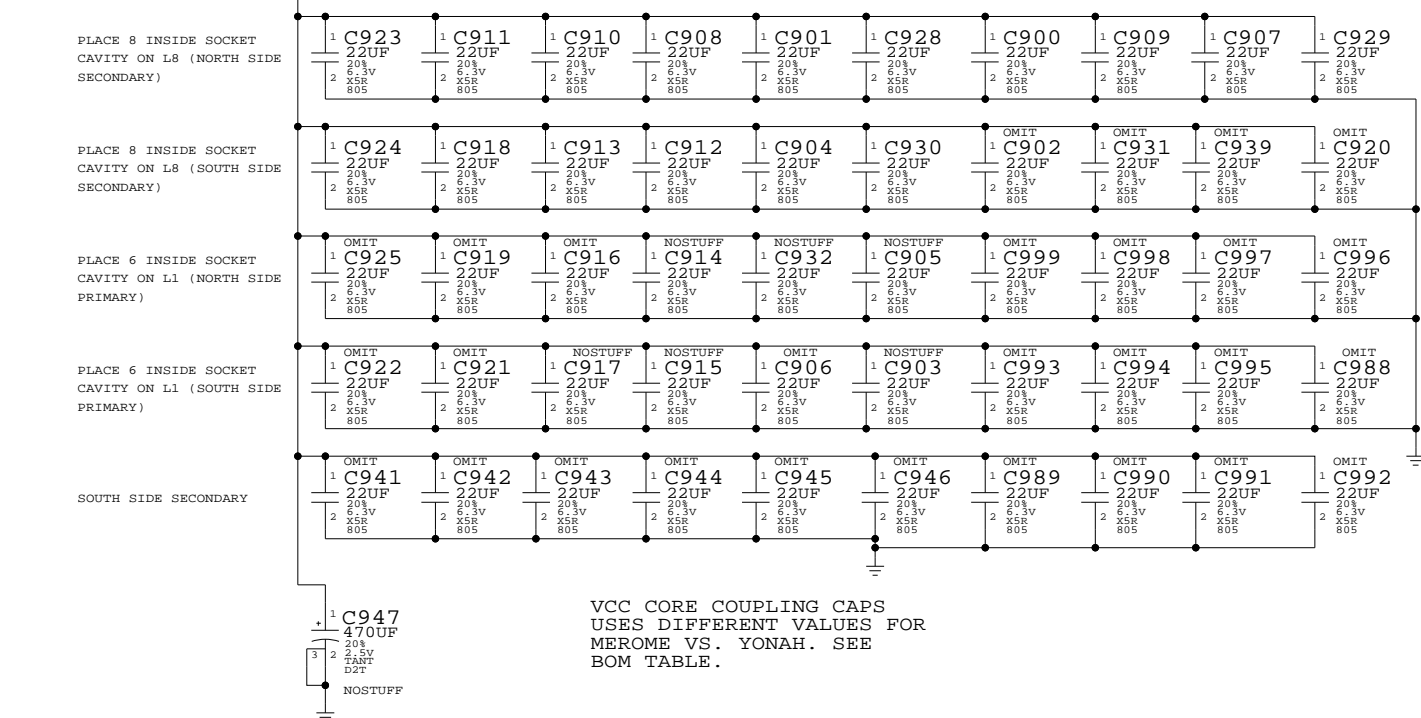
WE HAD A 330UF ELEC CAP HERE FOR 1.05V RAIL - CHECK WE CAN REMOVE

VCCP CORE DECOUPLING

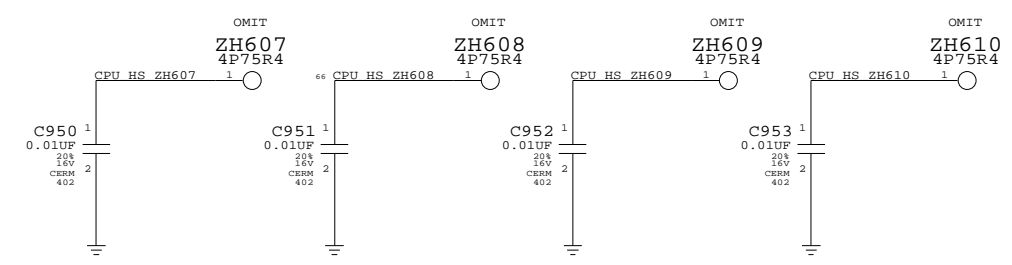


VCC CORE DECOUPLING

DESIGN FOR 44 CERAMIC AND 3 ELECT BULK 1800UF



CPU HEATSINK MOUNTING HOLES



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
138S0552	28	CAP, 22UF, 6.3V, 20%, X5R, 0805	C922, C925, C906, C939, C919, C993, C942, C991, C995		MEROME C990, C989, C988, C920, C997, C992, C994, C996, C921, C999, C943, C998, C944, C945, C946, C941, C916, C931, C902
138S0558	28	CAP, 10UF, 6.3V, 20%, X5R, 0805	C922, C925, C906, C939, C919, C993, C942, C991, C995		YONAH C990, C989, C988, C920, C997, C992, C994, C996, C921, C999, C943, C998, C944, C945, C946, C941, C916, C931, C902

CPU DECAPS & VID<>

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APPLE COMPUTER INC.

SCALE NONE SHEET 9 OF 97

DRAWING NUMBER 051-7199

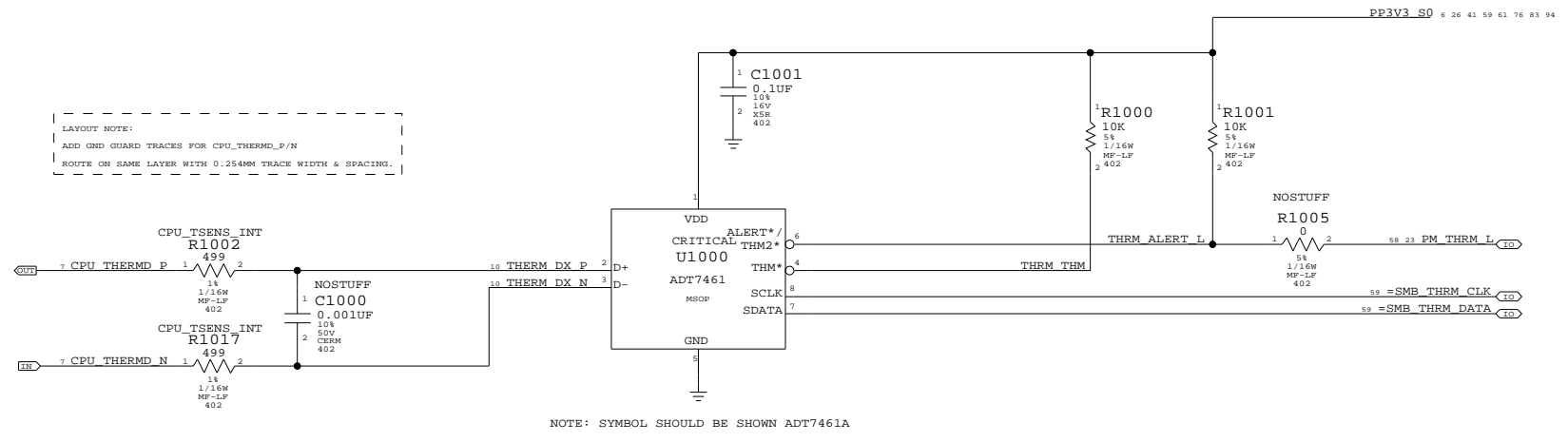
REV. E

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CPU THERMAL SENSOR

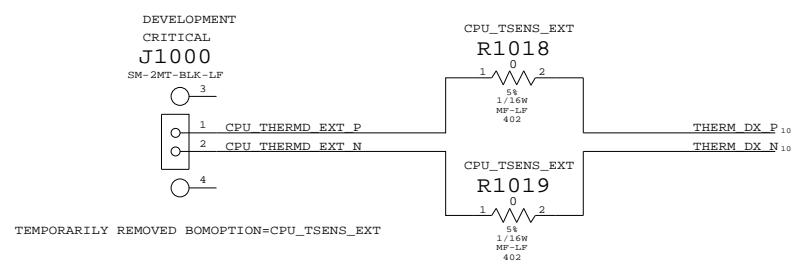
NOTE:
IF CPU T DIODE TO BE READ IN OFF STATE,
THEN THIS SHOULD BE S5

LAYOUT NOTE:
ADD GND GUARD TRACKS FOR CPU_THERMD_P/N
ROUTE ON SAME LAYER WITH 0.254MM TRACE WIDTH & SPACING.



NOTE: SYMBOL SHOULD BE SHOWN ADT7461A

LAYOUT NOTE:
PLACE R1002 AND R1018 SUCH THAT THEY SHARE ONE PAD
PLACE R1017 AND R1019 SUCH THAT THEY SHARE ONE PAD



CPU TEMP SENSOR

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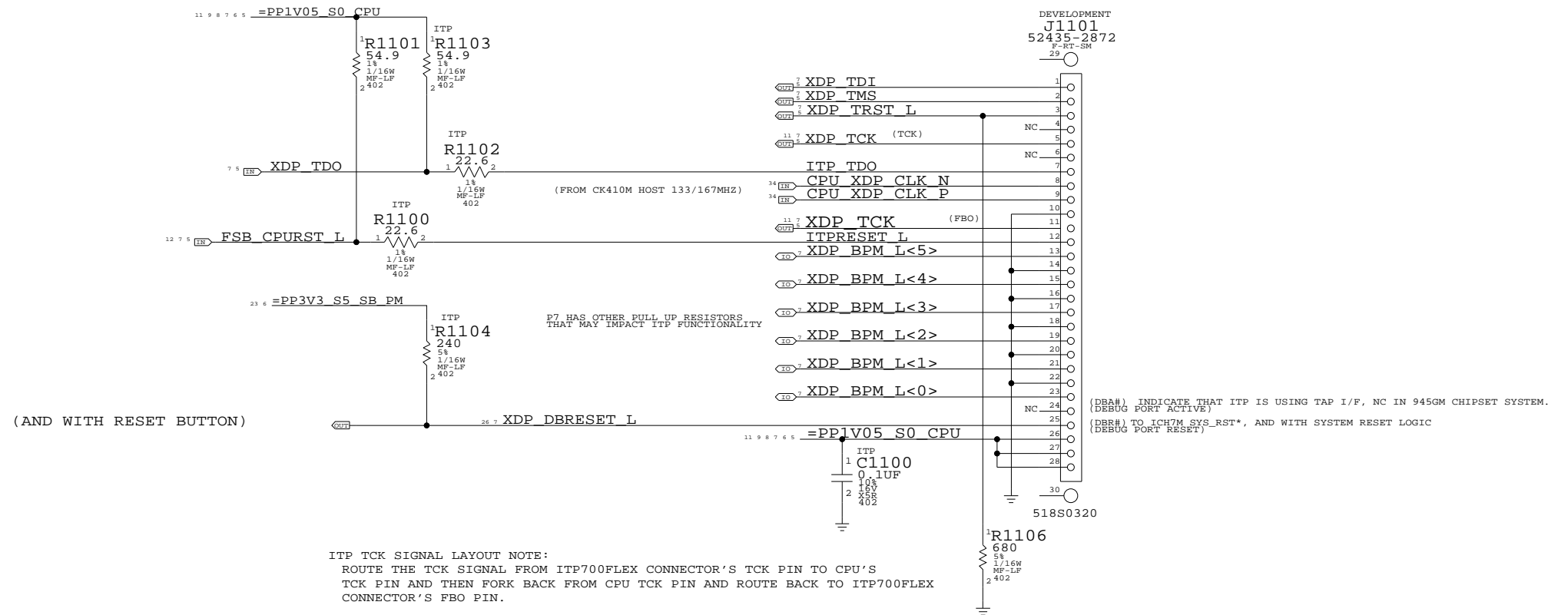
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	D	051-7199	E
SCALE	SHT	10 OF 97	
NONE			

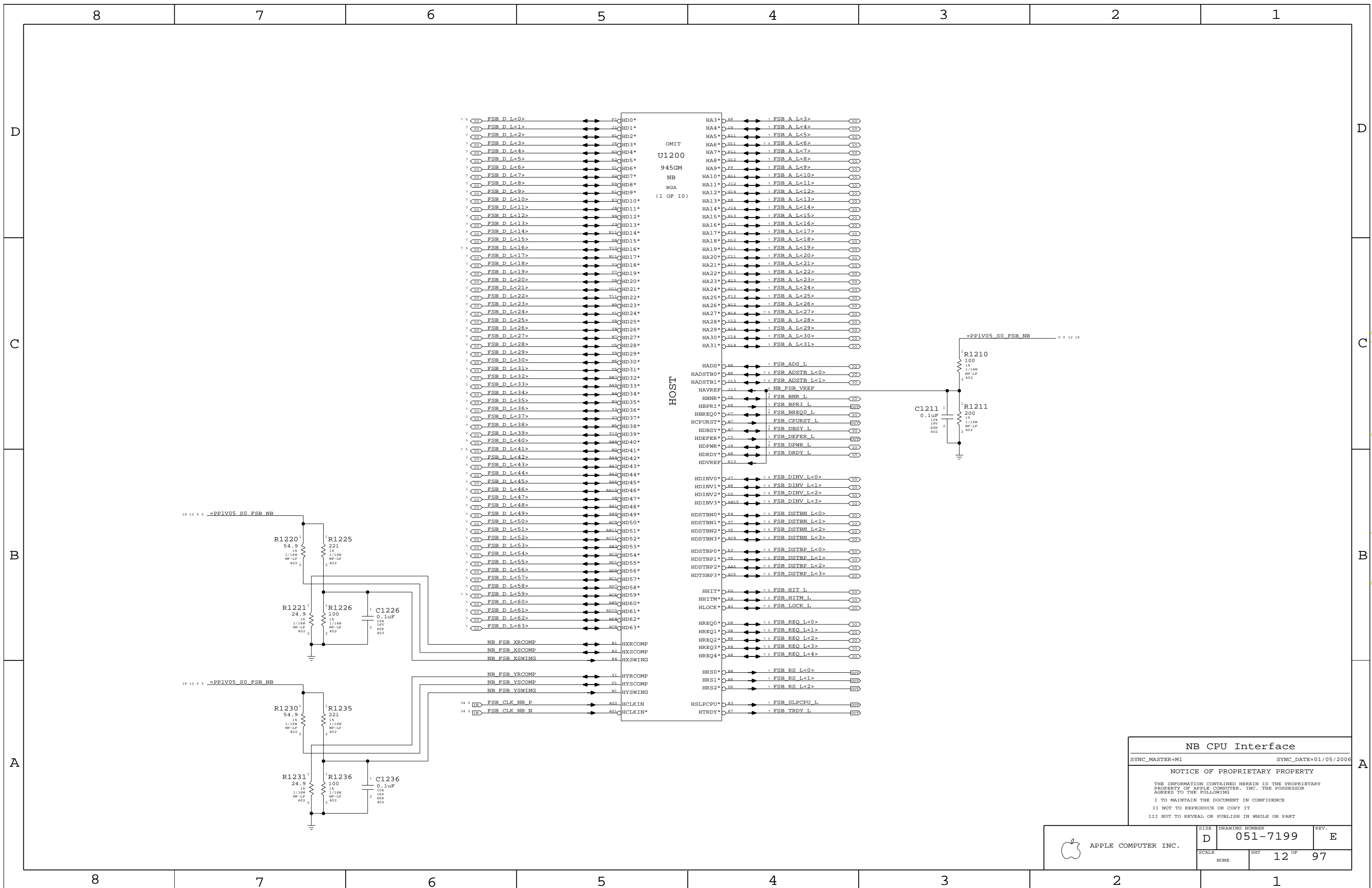
CPU ITP700FLEX DEBUG SUPPORT



CPU ITP700FLEX DEBUG
 SYNC_MASTER=M38 SYNC_DATE=01/05/2006

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	D	051-7199	E
SCALE	SHT	11 OF	97
NONE			



NB CPU Interface

SYNC_MASTER=M1 SYNC_DATE=01/05/2006

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	SCALE NONE	SHEET 12 OF 97	

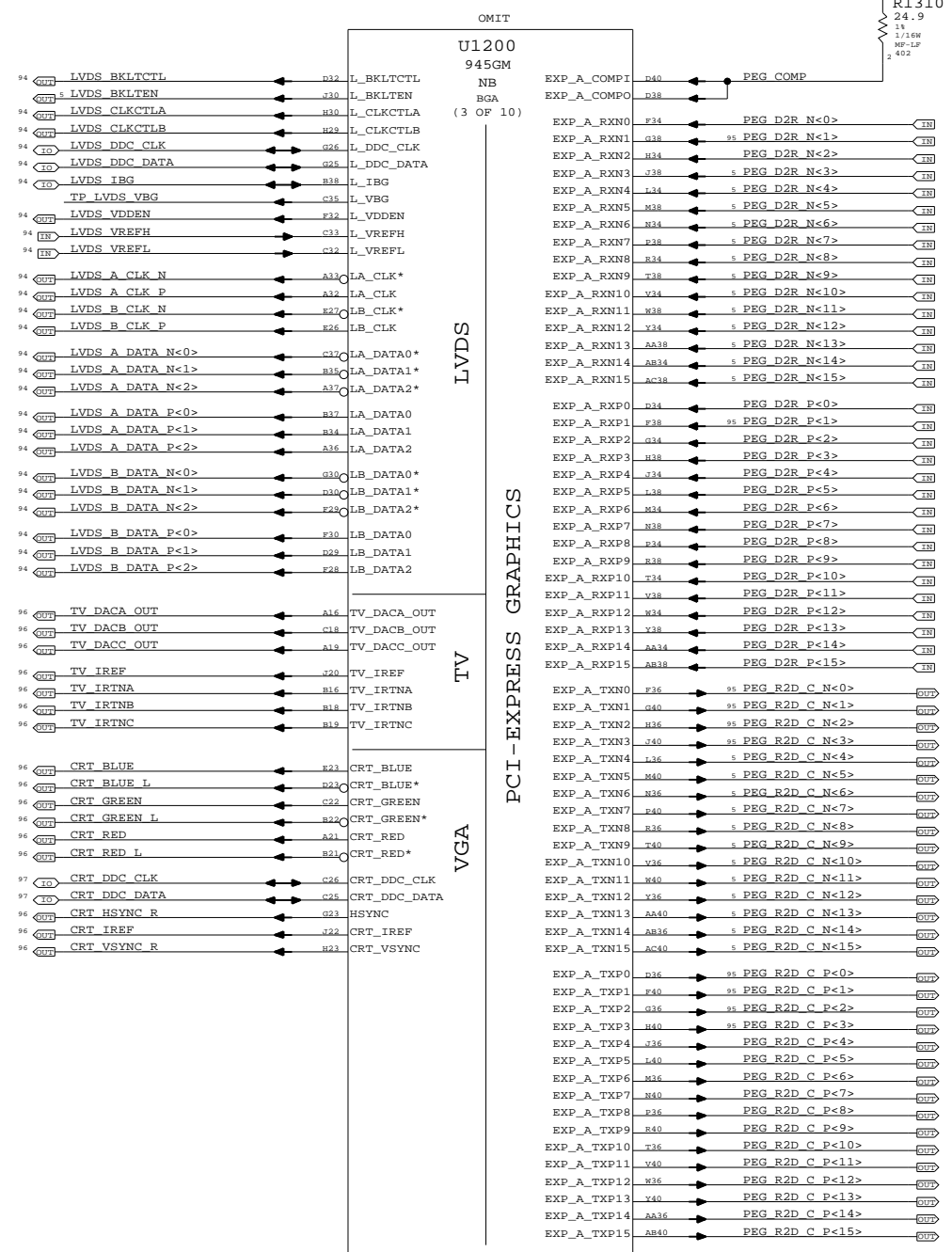
LVDS Disable
 Can leave all signals NC if LVDS is not implemented
 Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
 VCCD_LVDS must remain powered with proper decoupling.
 Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:
 Composite: DACA only
 S-Video: DACB & DACC only
 Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit
 filtering components. Unused DAC outputs should
 connect to GND through 75-ohm resistors.

TV-Out Disable
 Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail.
 Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and
 VCCA_TVVBG to 1.5V power rail. Tie VSSA_TVVBG to GND.

CRT Disable
 Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie
 HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core
 rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.



SDVO Alternate Function

SDVO_TVCLKIN#
 SDVO_INT#
 SDVO_FLDSTALL#

SDVO_TVCLKIN
 SDVO_INT
 SDVO_FLDSTALL

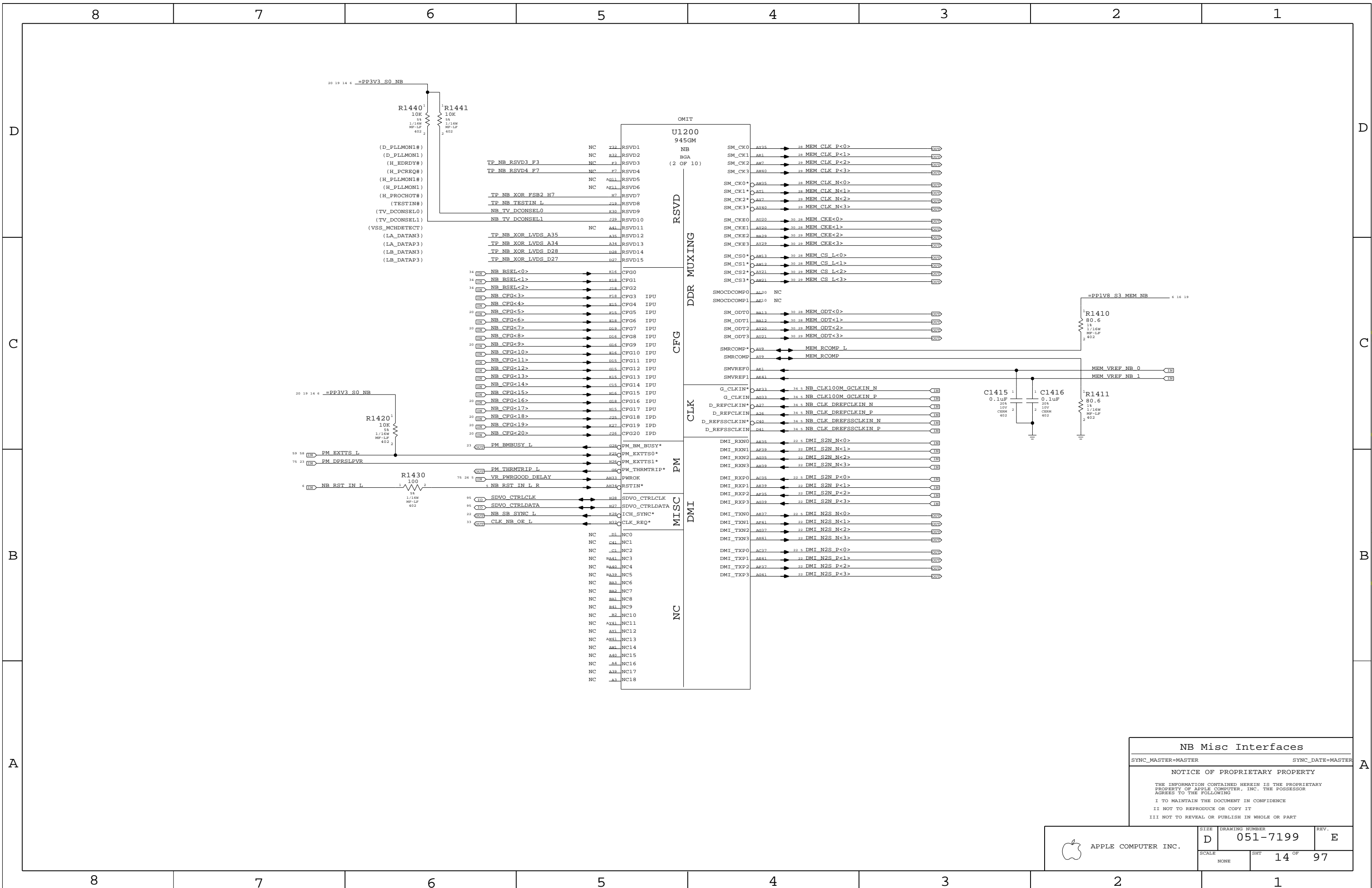
SDVOB_RED#
 SDVOB_GREEN#
 SDVOB_BLUE#
 SDVOB_CLKN
 SDVOC_RED#
 SDVOC_GREEN#
 SDVOC_BLUE#
 SDVOC_CLKN

SDVOB_RED
 SDVOB_GREEN
 SDVOB_BLUE
 SDVOB_CLKP
 SDVOC_RED
 SDVOC_GREEN
 SDVOC_BLUE
 SDVOC_CLKP

NB PEG / Video Interfaces
 SYNC_MASTER=M1 SYNC_DATE=01/05/2006

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	D	051-7199	E
SCALE	SHT	13 OF 97	
NONE			



NB Misc Interfaces

SYNC_MASTER=MASTER SYNC_DATE=MASTER

NOTICE OF PROPRIETARY PROPERTY

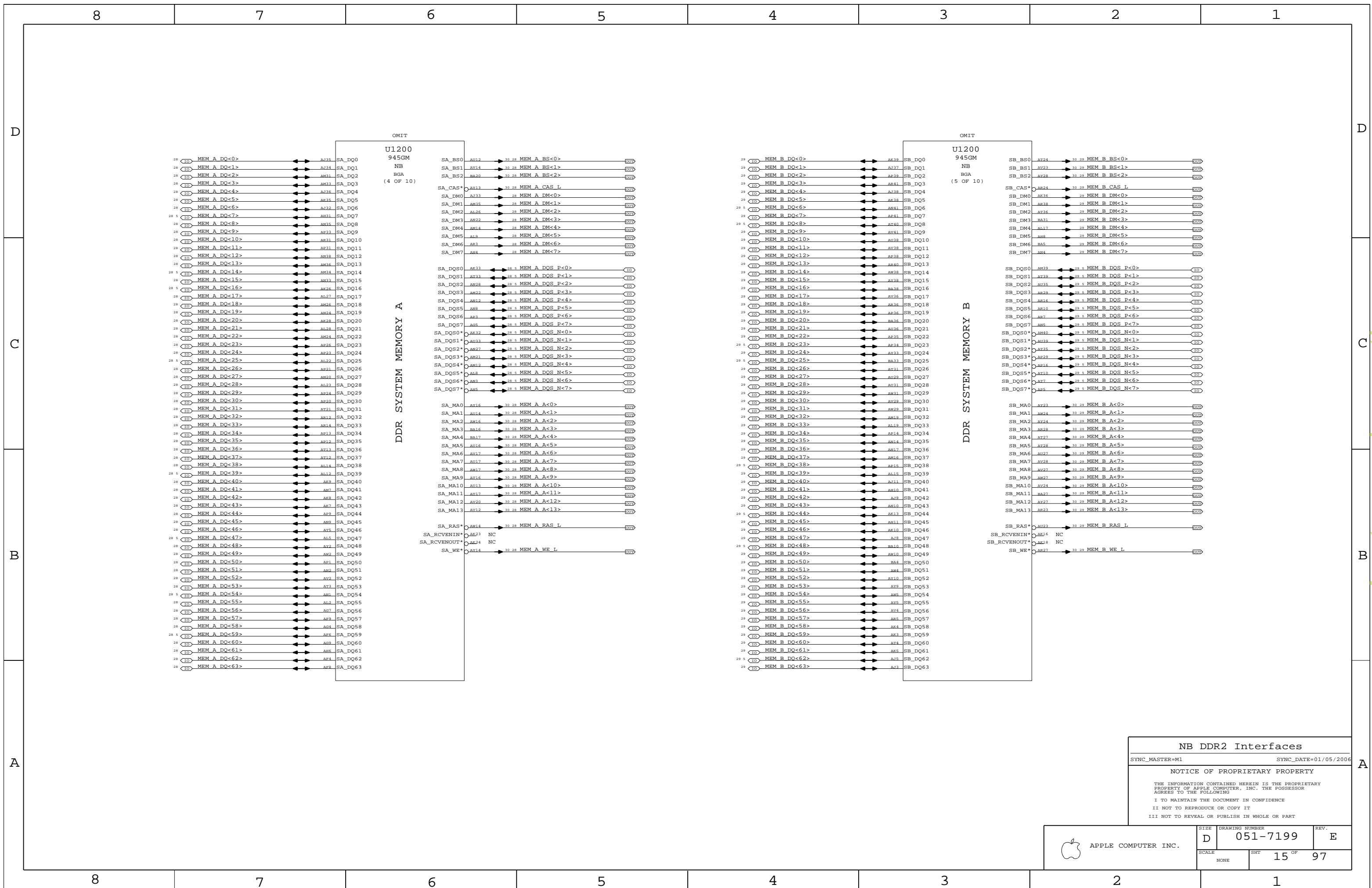
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	SCALE NONE	SHEET 14 OF 97	

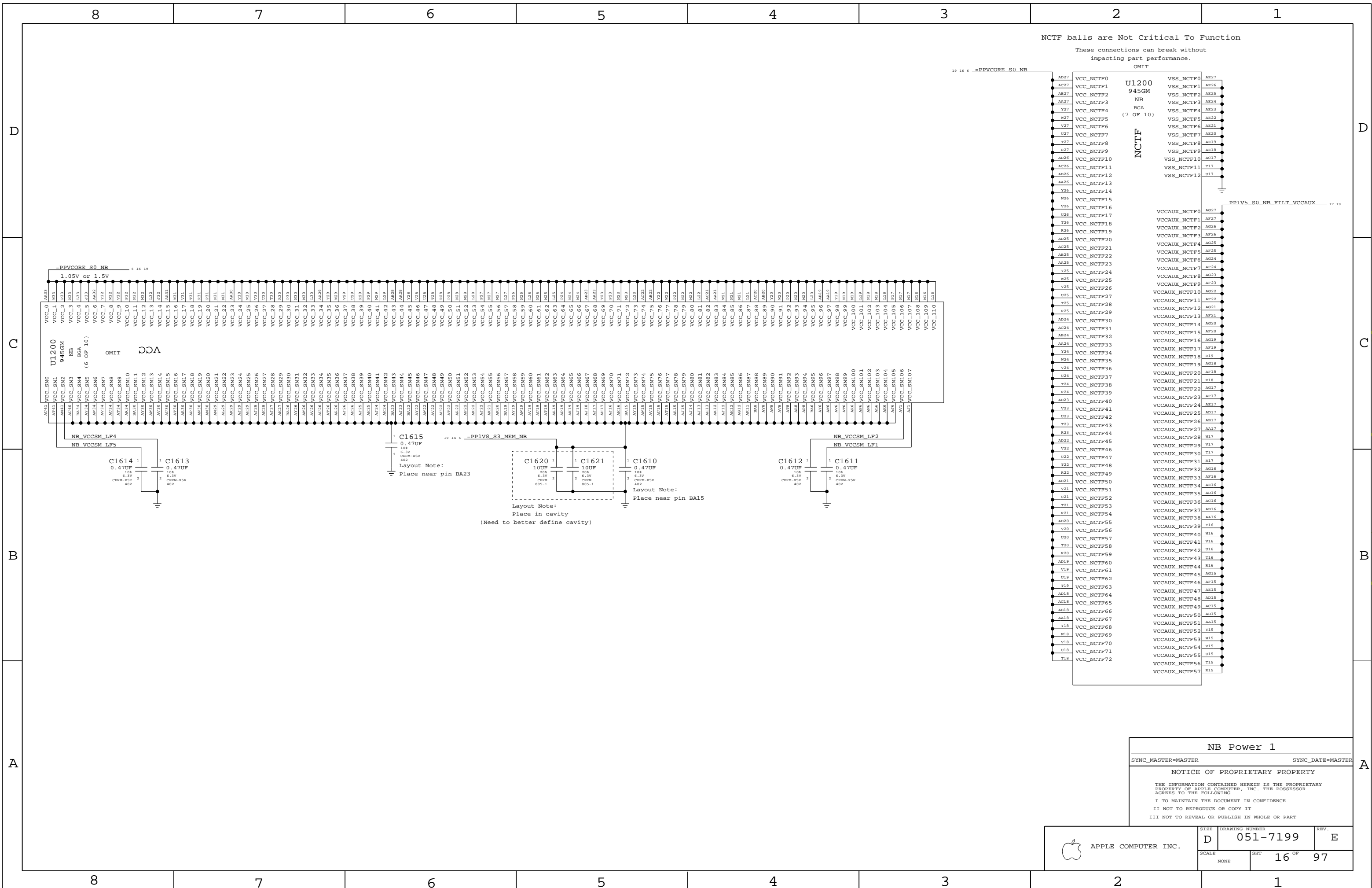


U1200 945GM NB BGA (4 OF 10)
 DDR SYSTEM MEMORY A

U1200 945GM NB BGA (5 OF 10)
 DDR SYSTEM MEMORY B

NB DDR2 Interfaces
 SYNC_MASTER=M1 SYNC_DATE=01/05/2006
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	SCALE: NONE	SHEET: 15 OF 97	



NB Power 1

SYNC_MASTER=MASTER SYNC_DATE=MASTER

NOTICE OF PROPRIETARY PROPERTY

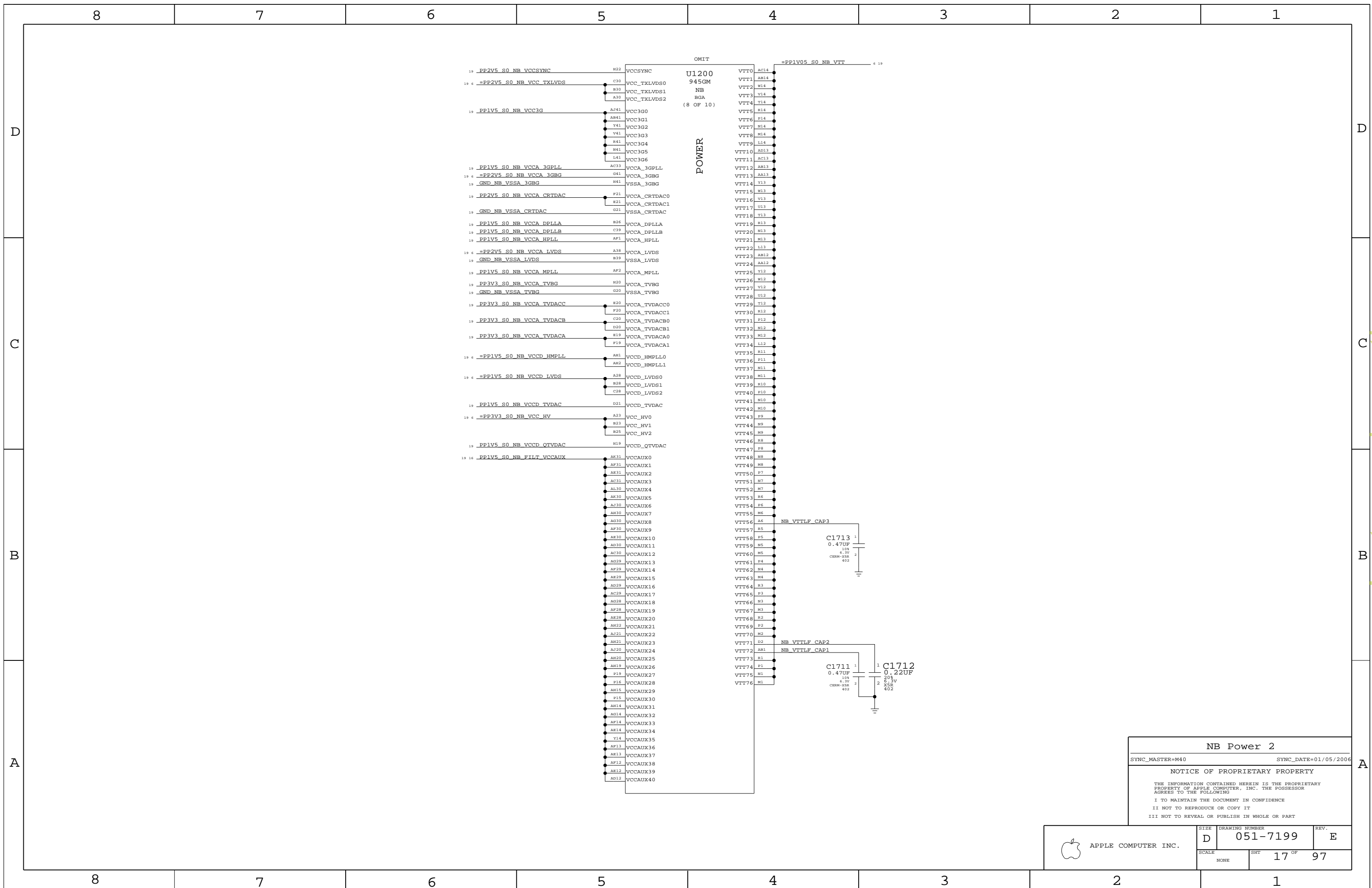
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7199	REV. E
	SCALE NONE	SHEET 16 OF 97	



NB Power 2

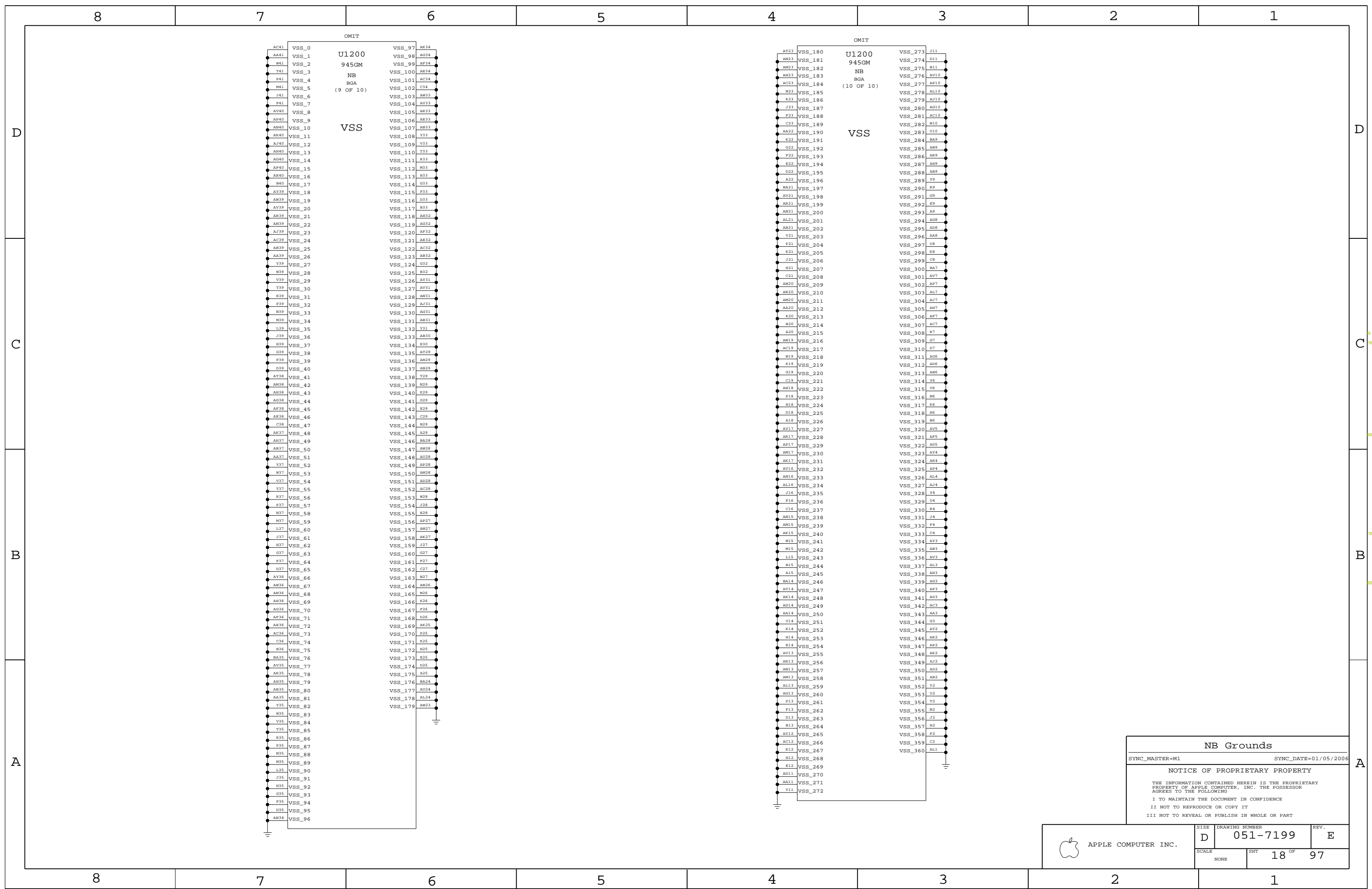
SYNC_MASTER=M40 SYNC_DATE=01/05/2006

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	SCALE NONE	SHEET 17 OF 97	



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NB Grounds

SYNC_MASTER=M1 SYNC_DATE=01/05/2006

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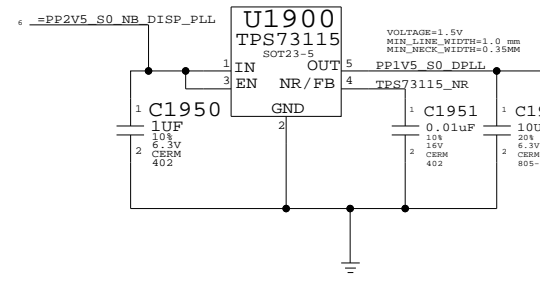
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	E
SCALE	SHT	18 OF 97	
NONE			

Power Interface

These are the power signals that leave the NB "block"

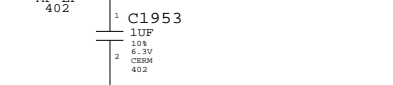
- =PP1V05_S0_FSB_NB 5 6 12
- =PPVCORE_S0_NB 6 16 19
- =PP1V05_S0_NB_VTT 6 17 19
- =PP1V5_S0_NB 6 19
- =PP1V5_S0_NB_PCIE 6 13
- =PP1V5_S0_NB_PLL 6 19
- =PP1V5_S0_NB_TVDAC 6 19
- =PP1V5_S0_NB_VCCD_HMPLL 6 17
- =PP1V5_S0_NB_VCCD_LVDS 6 17 19
- =PP1V5_S0_NB_VCCAUX 6 19
- =PP1V8_S3_MEM_NB 6 14 16 19
- =PP2V5_S0_NB_VCCSYNC 19 6
- =PP2V5_S0_NB_VCC_TLXVDS 6 17 19
- =PP2V5_S0_NB_VCCA_3BG 6 17 19
- =PP2V5_S0_NB_VCCA_LVDS 6 17 19
- =PP3V3_S0_NB 6 14 20
- =PP3V3_S0_NB_VCC_HV 6 17 19
- =PP5V_S0_NB_TVDAC 6 19

MCH DISPLAY PLL POWER LDO



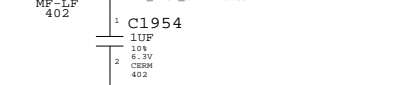
MCH VCCA_DPLL FILTER

(MCH DISPLAY A PLL 1.5V PWR)



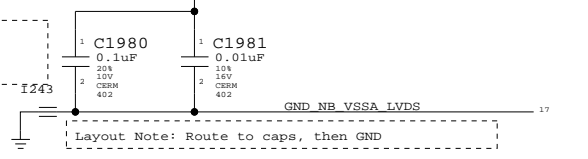
GMCH VCCA_DPLL_B FILTER

(MCH DISPLAY B PLL 1.5V PWR)



MCH VCCA_LVDS FILTER

(MCH LVDS ANALOG 2.5V PWR)



GMCH VCCD_LVDS BYPASS

(MCH LVDS DIGITAL 1.5V PWR)



GMCH VCCD_LVDS BYPASS

(MCH LVDS DIGITAL TX 2.5V PWR)



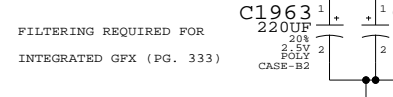
MCH VCCSYNC BYPASS

(MCH H/V SYNC 2.5V PWR)



GMCH VCCD_LVDS BYPASS

(MCH LVDS DIGITAL TX 2.5V PWR)



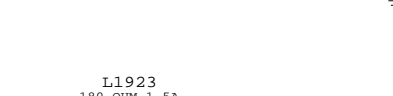
GMCH VCCD_LVDS BYPASS

(MCH LVDS DIGITAL TX 2.5V PWR)



GMCH VCCD_LVDS BYPASS

(MCH LVDS DIGITAL TX 2.5V PWR)



GMCH VCCD_TVDAC FILTER

(MCH TVDAC DEDICATED PWR 1.5V)



GMCH VCCD_QTVDAC FILTER

(MCH TVDAC DIGITAL QUIET 1.5V PWR)



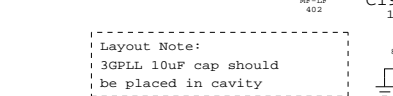
GMCH VCCD_QTVDAC FILTER

(MCH TVDAC DIGITAL QUIET 1.5V PWR)



GMCH VCCD_QTVDAC FILTER

(MCH TVDAC DIGITAL QUIET 1.5V PWR)



Layout Note:
This 0.1uF cap should be within 5 mm of NB edge

Layout Note:
Route to caps, then GND

Layout Note:
These 2 caps should be within 6.35 mm of NB edge

Layout Note:
Route to caps, then GND

Layout Note:
These 4 0.1uF caps should be within 5 mm of NB edge

Layout Note:
Place in cavity

Layout Note:
Place on the edge

Layout Note:
PLACE CAPS NEAR NB EDGE ON THESE 2 RAILS

Layout Note:
These 8 caps should be within 6.35 mm of NB edge

Layout Note:
10uF caps should be close to MCH on opposite side.

Layout Note:
Route to caps, then GND

Layout Note:
Place L and C close to MCH

Layout Note:
3GPLL 10uF cap should be placed in cavity

Layout Note:
Route to caps, then GND

NB (GM) Decoupling

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

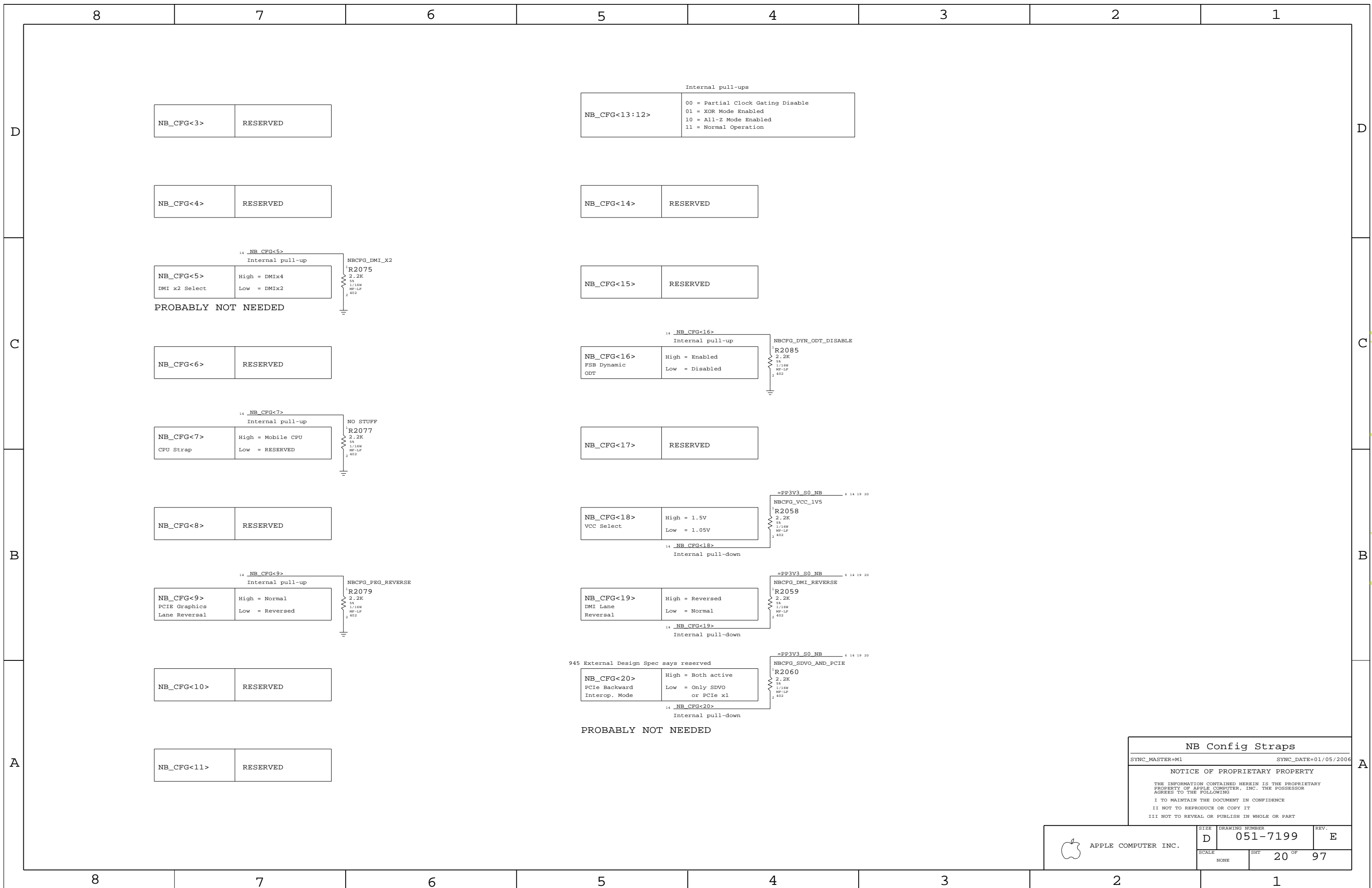
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	D	051-7199	E
SCALE	SHT	19 OF 97	
NONE			



Internal pull-ups

NB_CFG<13:12>	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation
---------------	--

NB_CFG<14>	RESERVED
------------	----------

NB_CFG<15>	RESERVED
------------	----------

Internal pull-up

NB_CFG<16>	High = Enabled Low = Disabled
------------	----------------------------------

Internal pull-down

NB_CFG<17>	RESERVED
------------	----------

Internal pull-down

NB_CFG<18>	High = 1.5V Low = 1.05V
------------	----------------------------

Internal pull-down

NB_CFG<19>	High = Reversed Low = Normal
------------	---------------------------------

Internal pull-down

NB_CFG<20>	High = Both active Low = Only SDVO or PCIe x1 Interop. Mode
------------	--

NB_CFG<3>	RESERVED
-----------	----------

NB_CFG<4>	RESERVED
-----------	----------

Internal pull-up

NB_CFG<5>	High = DMIX4 Low = DMIX2
-----------	-----------------------------

PROBABLY NOT NEEDED

NB_CFG<6>	RESERVED
-----------	----------

Internal pull-up

NB_CFG<7>	High = Mobile CPU Low = RESERVED
-----------	-------------------------------------

NB_CFG<8>	RESERVED
-----------	----------

Internal pull-up

NB_CFG<9>	High = Normal Low = Reversed
-----------	---------------------------------

NB_CFG<10>	RESERVED
------------	----------

NB_CFG<11>	RESERVED
------------	----------

NB Config Straps

SYNC_MASTER=M1 SYNC_DATE=01/05/2006

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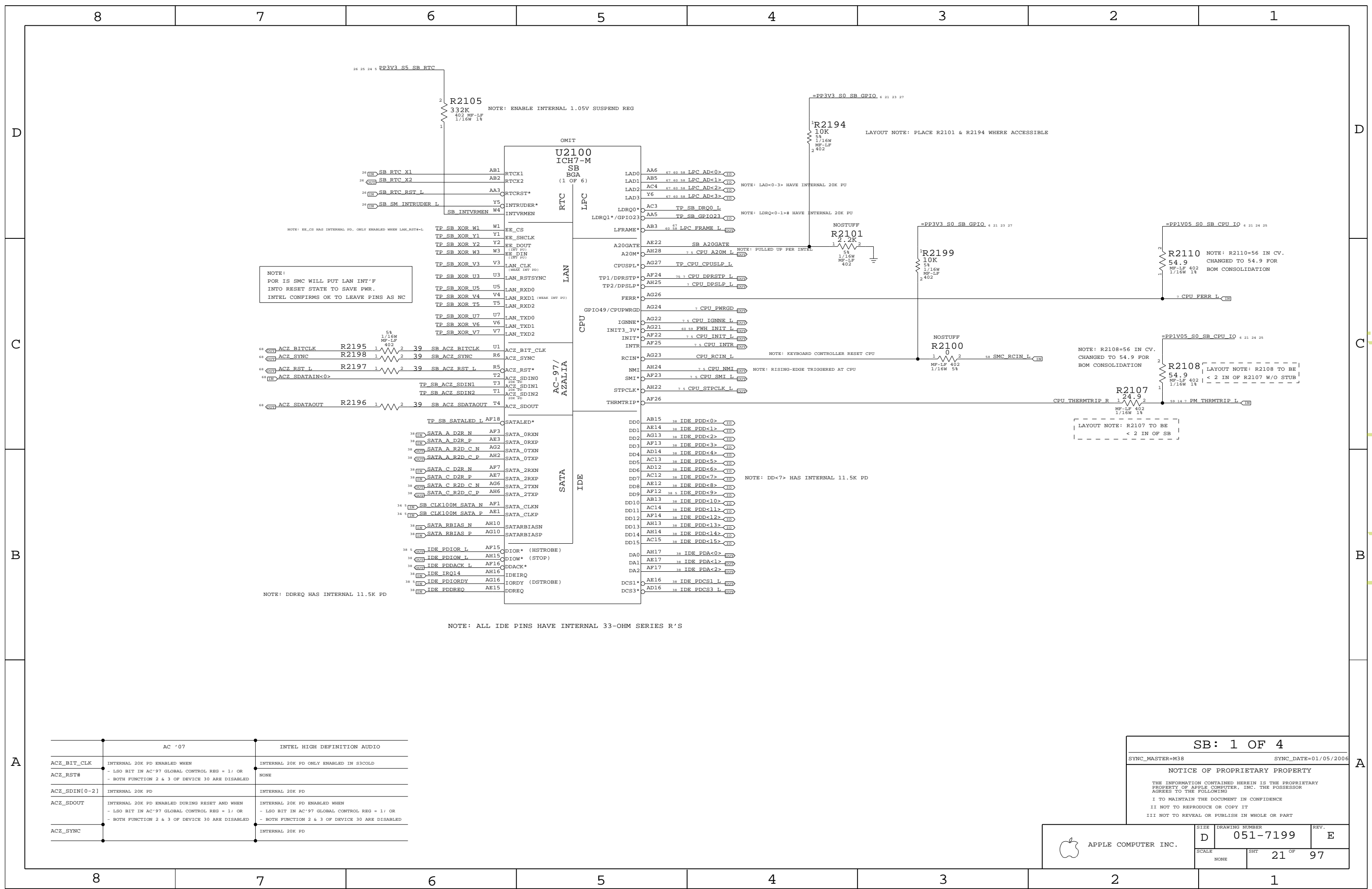
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	D	051-7199	E
SCALE	SHT	20 OF 97	
NONE			

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NOTE:
POR IS SMC WILL PUT LAN INT'F INTO RESET STATE TO SAVE PWR. INTEL CONFIRMS OK TO LEAVE PINS AS NC

AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR
ACZ_RST#	NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC	INTERNAL 20K PD

SB: 1 OF 4

SYNC_MASTER=M38 SYNC_DATE=01/05/2006

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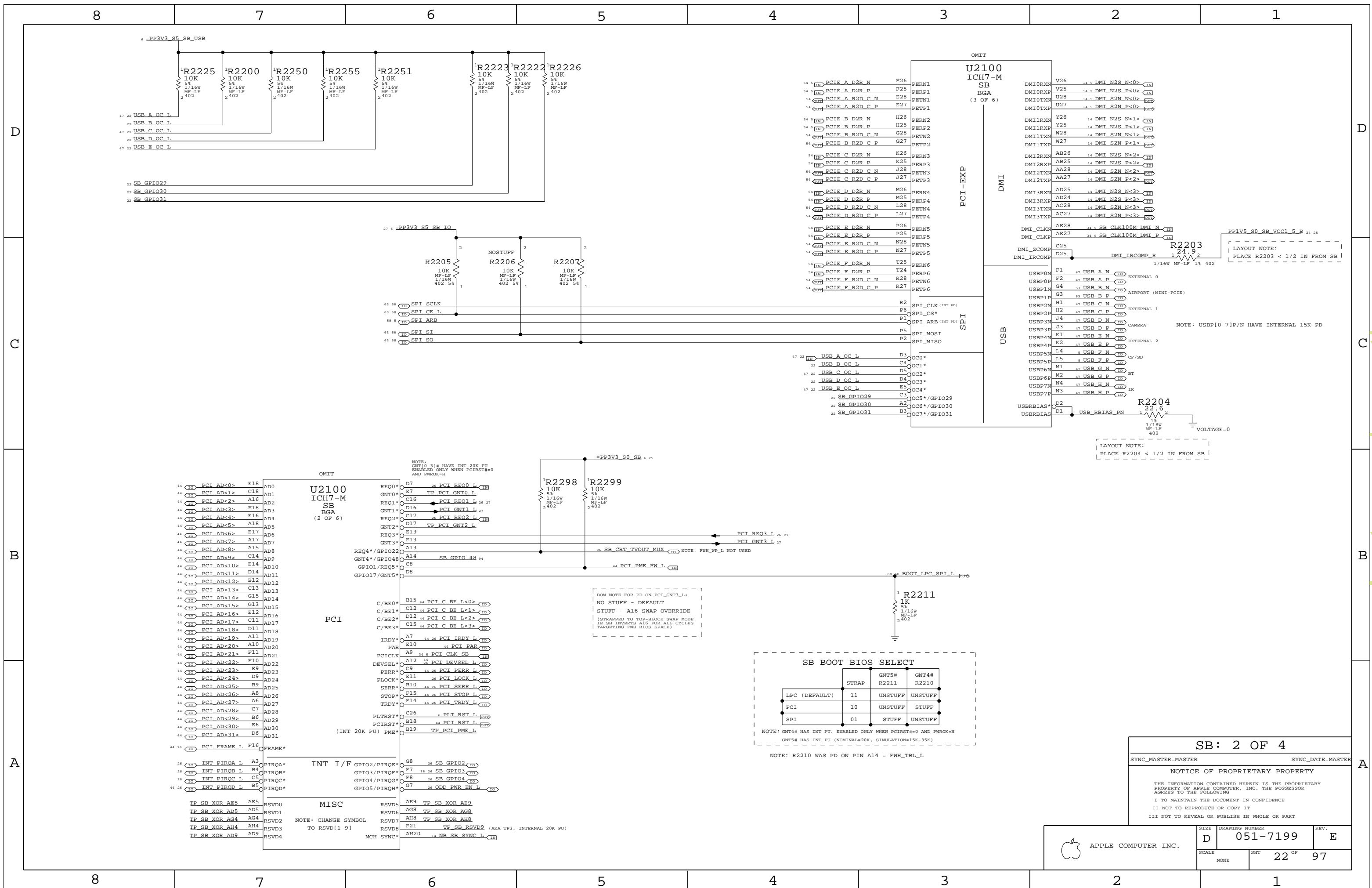
SCALE: NONE

DRAWING NUMBER: D 051-7199

SHT: 21 OF 97

REV: E

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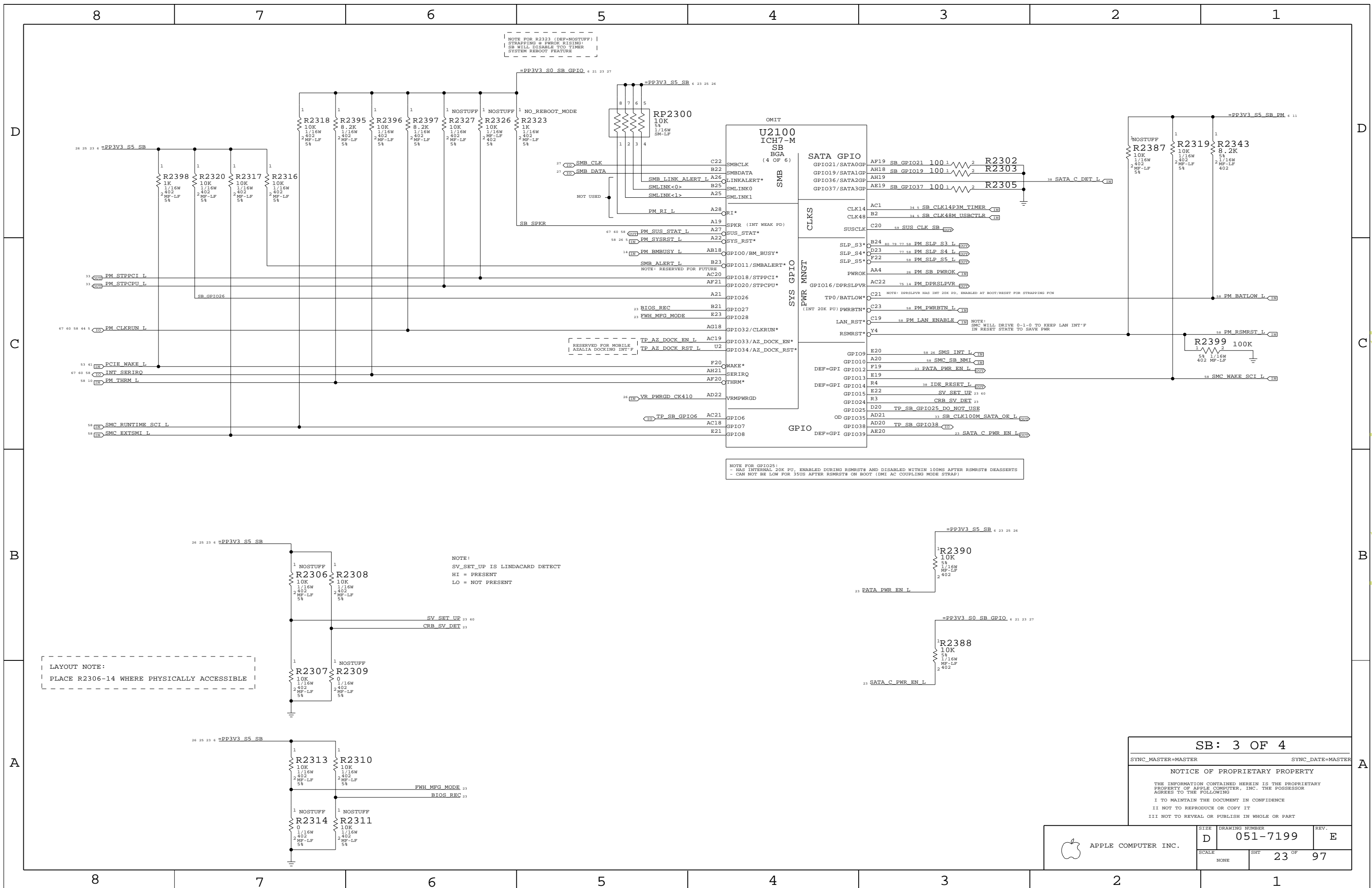
SB: 2 OF 4

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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	NONE	051-7199	E
SHEET		22 OF 97	



NOTE FOR R2323 (DEF-NOSTUFF) | STRAPPING # PWROK RISING: SB WILL DISABLE TCO TIMER SYSTEM REBOOT FEATURE

NOTE FOR GPIO25:
 - HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS
 - CAN NOT BE LOW FOR 35US AFTER RSMRST# ON BOOT (DMI AC COUPLING MODE STRAP)

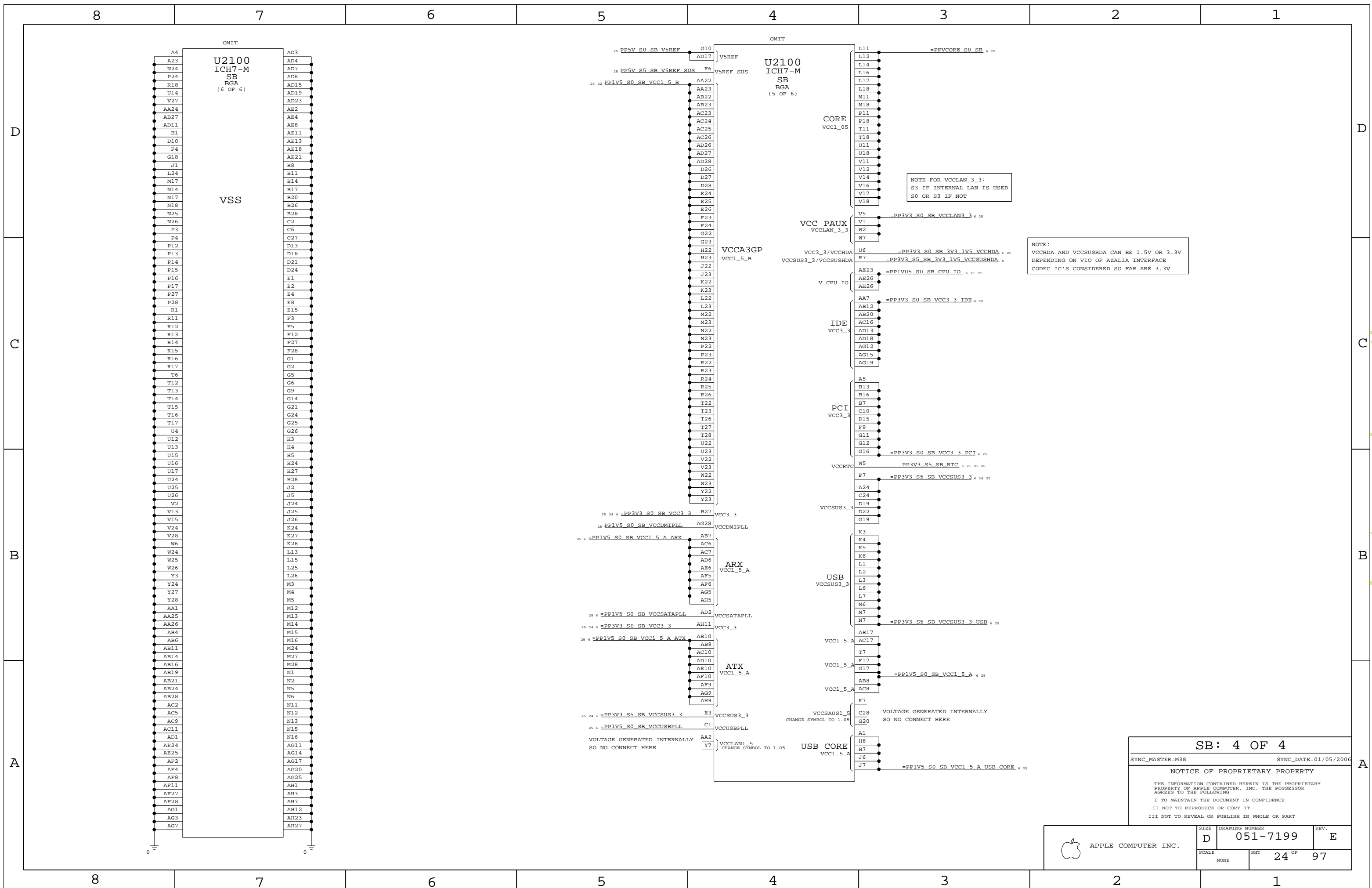
LAYOUT NOTE:
 PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

NOTE:
 SV_SET_UP IS LINDACARD DETECT
 HI = PRESENT
 LO = NOT PRESENT

SB: 3 OF 4
 SYNC_MASTER=MASTER SYNC_DATE=MASTER
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SCALE	NONE	SHT	23 OF 97

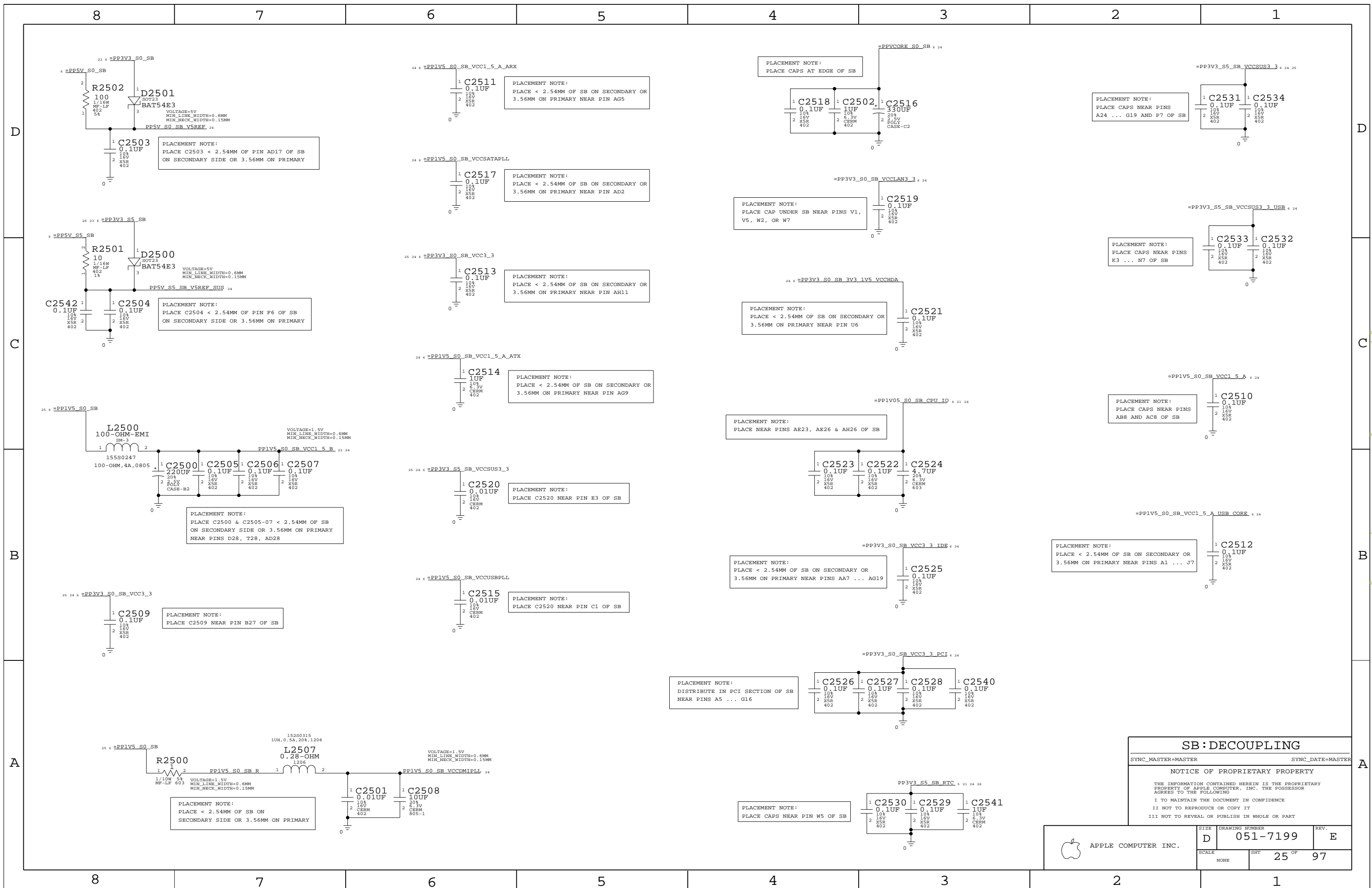
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SB: 4 OF 4
 SYNC_MASTER=M38 SYNC_DATE=01/05/2006
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	D	051-7199	E
SCALE	SHT	24 OF 97	
NONE			



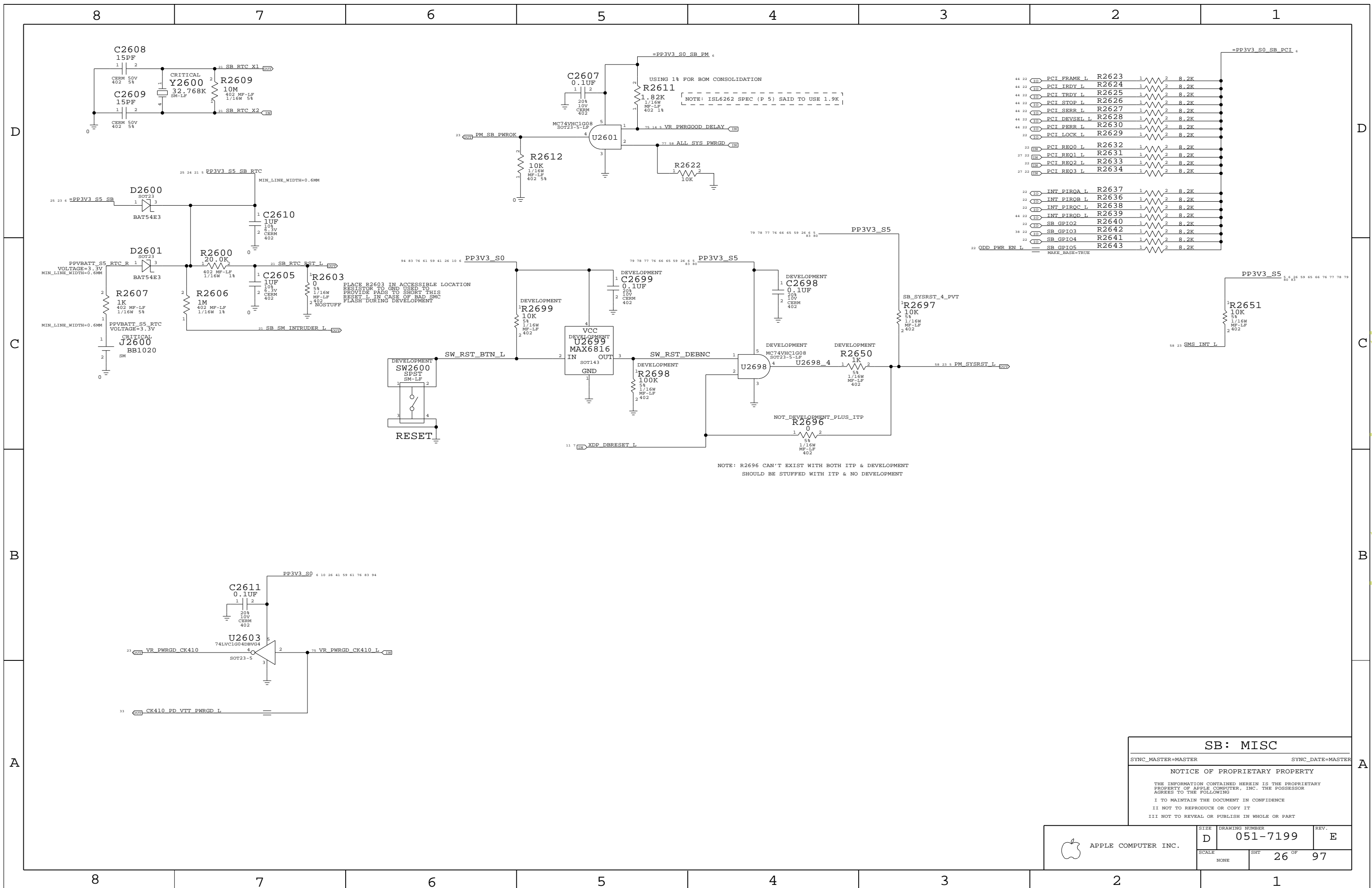
SB: DECOUPLING

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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SCALE	SHT	25 OF	97
NONE			



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SB: MISC
 SYNC_MASTER=MASTER SYNC_DATE=MASTER
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	D	051-7199	E
SCALE	SHT	26 OF	97
NONE			

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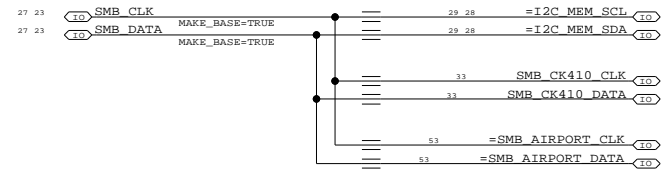
B

B

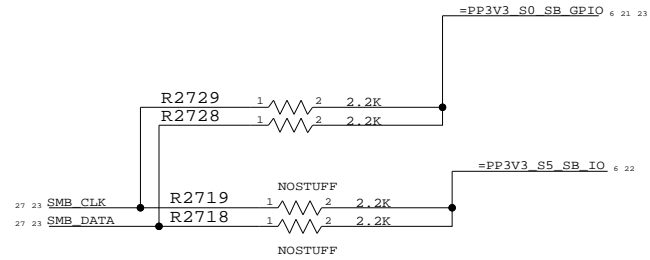
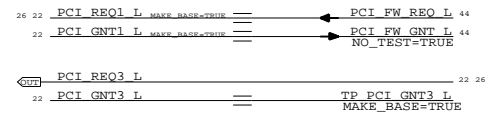
A

A

SB I2C BUSSES



PCI CONTROL



SB: SMB HUB AND ALIAS

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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	D	051-7199	E
SCALE	SHT	27 OF 97	
NONE			

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Page Notes

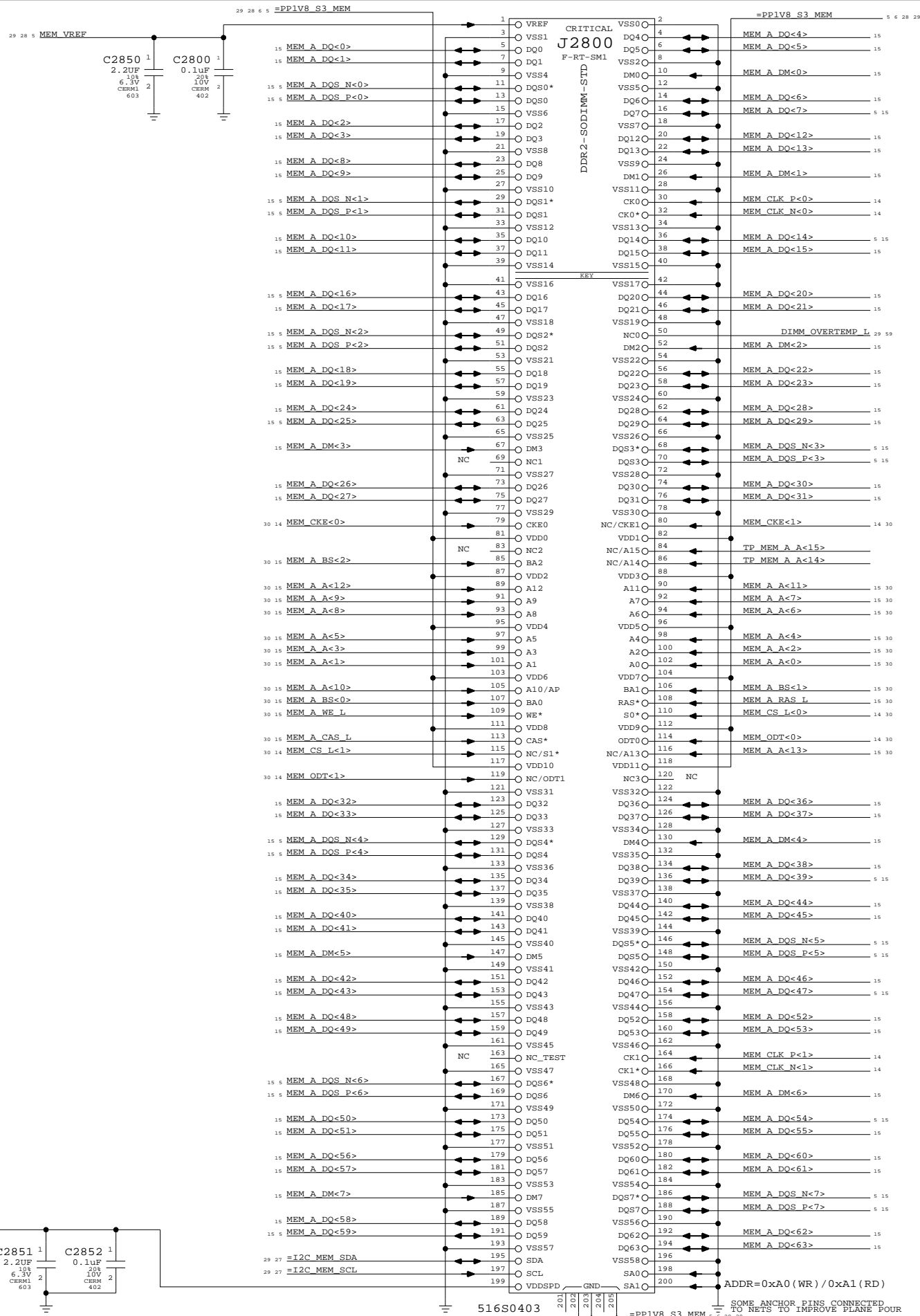
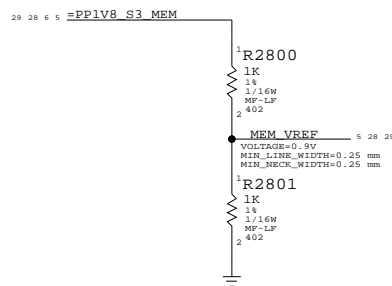
Power aliases required by this page:
 - =PPIV8_S3_MEM
 - =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
 - =I2C_MEM_SCL
 - =I2C_MEM_SDA

BOM options provided by this page:
 (NONE)

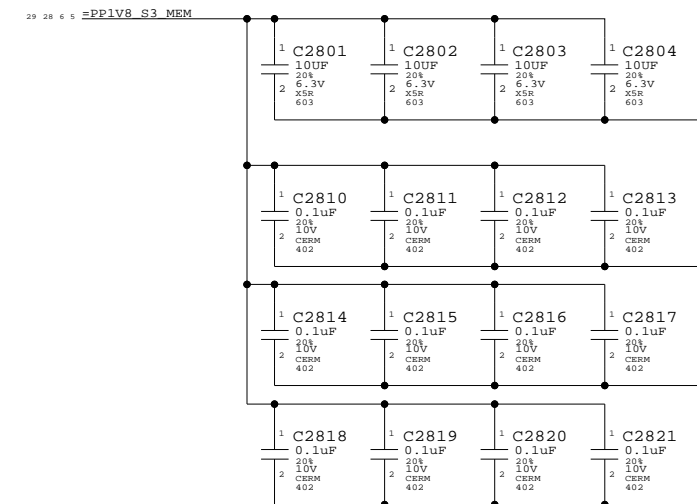
DDR2 VRef

One 0.1uF per connector



DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector A

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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	SCALE NONE	SHEET 28 OF 97	

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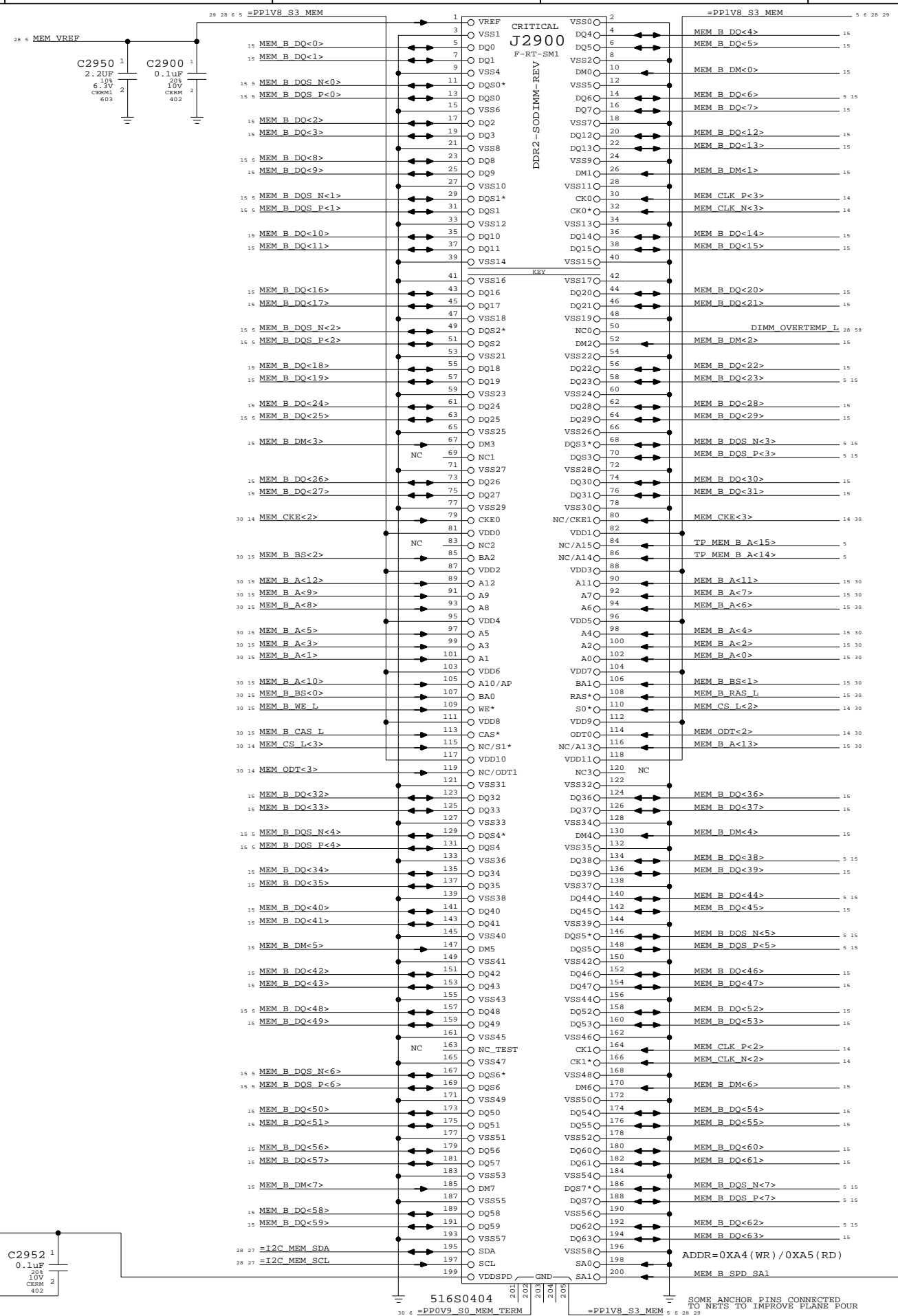
Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

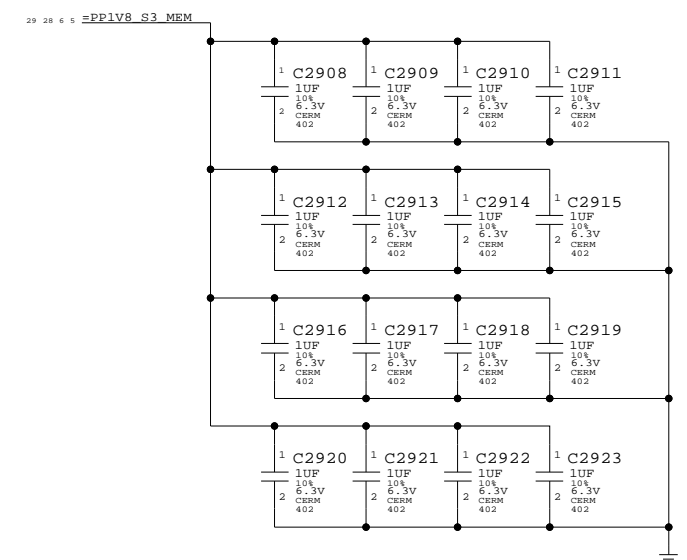
Signal aliases required by this page:
- =I2C_MEM_SCL
- =I2C_MEM_SDA

BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF.
The reference voltage must be provided by another page.



DDR2 Bypass Caps (For return current)



DDR2 SO-DIMM Connector B	
SYNC_MASTER=MASTER	SYNC_DATE=MASTER
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	D	051-7199	E
SCALE	SHT	29 OF	97
NONE			

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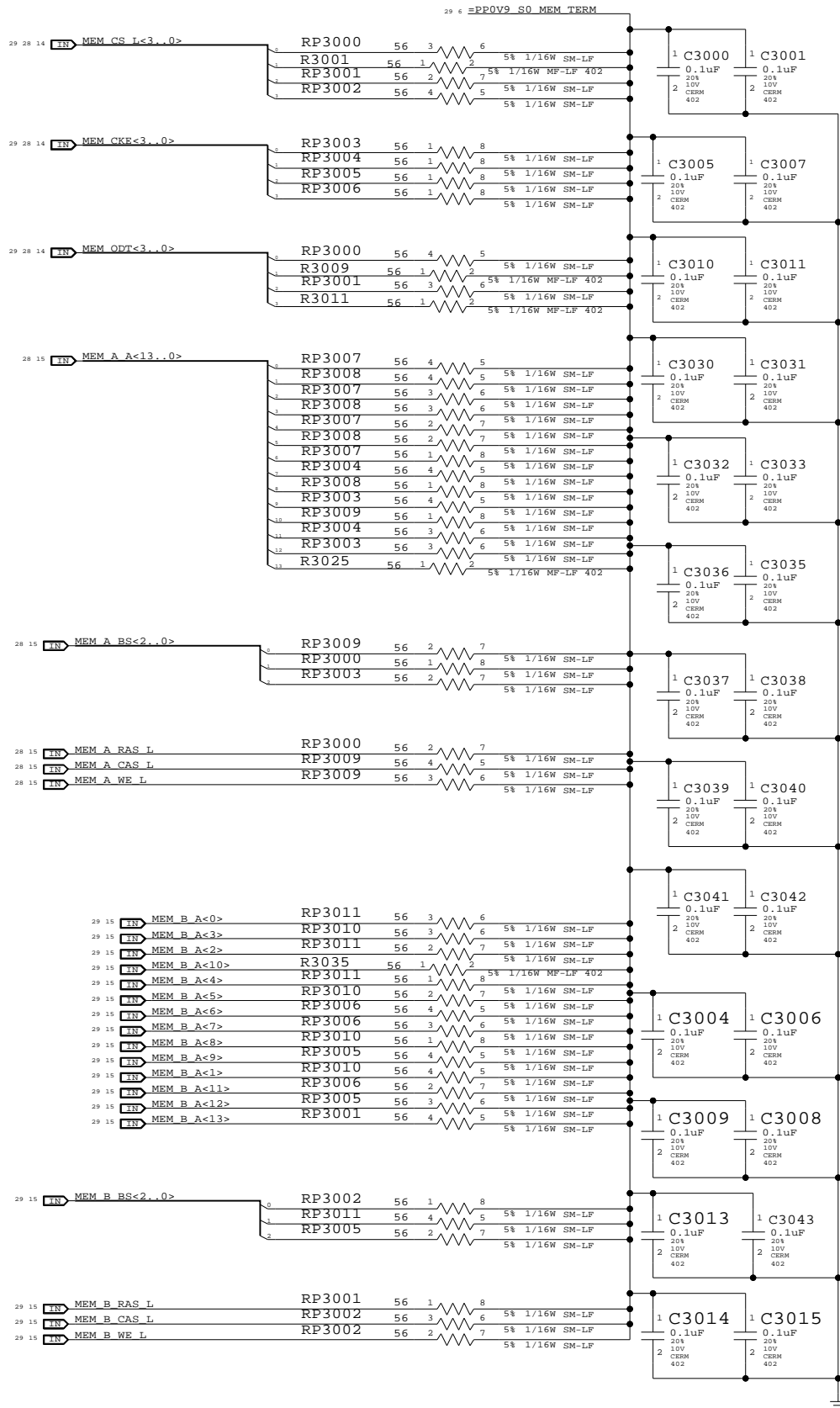
4

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One cap for each side of every RPAK, one cap for every two discrete resistors
BOMOPTION shown at the top of each group applies to every part below it



Memory Active Termination

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	D	051-7199	E
SCALE	SHT	30 OF 97	
NONE			

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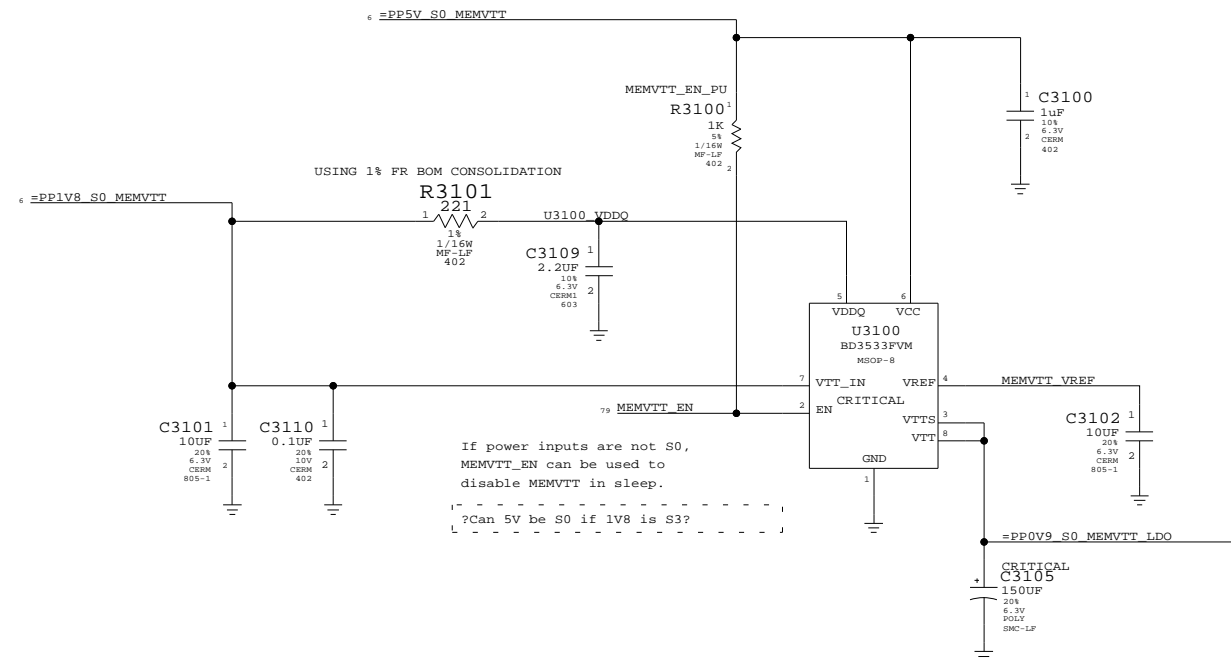
Page Notes

Power aliases required by this page:
 - =PP5V_S0_MEMVTT
 - =PP1V8_S0_MEMVTT
 - =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
 (NONE)

BOM options provided by this page:
 (NONE)

DDR2 Vtt Regulator



Memory Vtt Supply

SYNC_MASTER=MASTER SYNC_DATE=MASTER

NOTICE OF PROPRIETARY PROPERTY

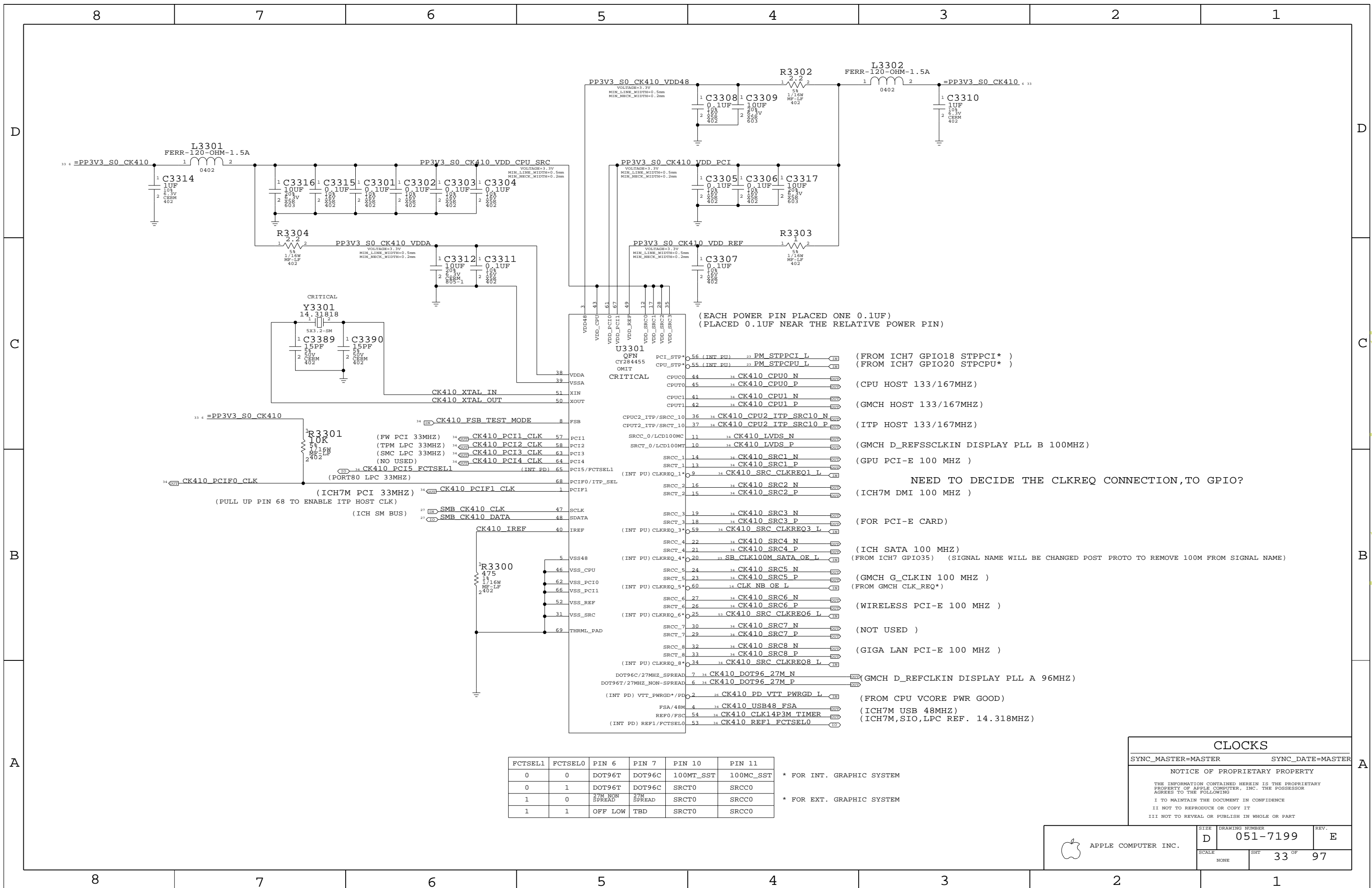
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	E
SCALE	SHT	31 OF 97	
NONE			



(EACH POWER PIN PLACED ONE 0.1UF)
(PLACED 0.1UF NEAR THE RELATIVE POWER PIN)

U3301
QFN
CY284455
CRITICAL

PCI_STP*	56 (INT PU)	23	PM_STPPCI L	(FROM ICH7 GPIO18 STPPCI*)
CPU_STP*	55 (INT PU)	23	PM_STPCPU L	(FROM ICH7 GPIO20 STPCPU*)
CPU0	44	34	CK410 CPU0 N	(CPU HOST 133/167MHZ)
CPU0 P	45	34	CK410 CPU0 P	
CPU1	41	34	CK410 CPU1 N	(GMCH HOST 133/167MHZ)
CPU1 P	42	34	CK410 CPU1 P	
CPU2_ITP/SRCC_10	36	34	CK410 CPU2 ITP_SRC10 N	(ITP HOST 133/167MHZ)
CPU2_ITP/SRCC_10	37	34	CK410 CPU2 ITP_SRC10 P	
SRCC_0/LCD100MC	11	34	CK410 LVDS N	(GMCH D_REFSSCLKIN DISPLAY PLL B 100MHZ)
SRCT_0/LCD100MT	10	34	CK410 LVDS P	
SRCC_1	14	34	CK410 SRC1 N	(GPU PCI-E 100 MHZ)
SRCT_1	13	34	CK410 SRC1 P	
(INT PU) CLKREQ_1*	9	34	CK410 SRC CLKREQ1 L	NEED TO DECIDE THE CLKREQ CONNECTION, TO GPIO?
SRCC_2	16	34	CK410 SRC2 N	(ICH7M DMI 100 MHZ)
SRCT_2	15	34	CK410 SRC2 P	
SRCC_3	19	34	CK410 SRC3 N	(FOR PCI-E CARD)
SRCT_3	18	34	CK410 SRC3 P	
(INT PU) CLKREQ_3*	59	34	CK410 SRC CLKREQ3 L	
SRCC_4	22	34	CK410 SRC4 N	(ICH SATA 100 MHZ)
SRCT_4	21	34	CK410 SRC4 P	(FROM ICH7 GPIO35) (SIGNAL NAME WILL BE CHANGED POST PROTO TO REMOVE 100M FROM SIGNAL NAME)
(INT PU) CLKREQ_4*	20	34	SB_CLK100M SATA OE L	
SRCC_5	24	34	CK410 SRC5 N	(GMCH G_CLKIN 100 MHZ)
SRCT_5	23	34	CK410 SRC5 P	(FROM GMCH CLK_REQ*)
(INT PU) CLKREQ_5*	60	34	CLK_NB OE L	
SRCC_6	27	34	CK410 SRC6 N	(WIRELESS PCI-E 100 MHZ)
SRCT_6	26	34	CK410 SRC6 P	
(INT PU) CLKREQ_6*	25	34	CK410 SRC CLKREQ6 L	
SRCC_7	30	34	CK410 SRC7 N	(NOT USED)
SRCT_7	29	34	CK410 SRC7 P	
SRCC_8	32	34	CK410 SRC8 N	(GIGA LAN PCI-E 100 MHZ)
SRCT_8	33	34	CK410 SRC8 P	
(INT PU) CLKREQ_8*	34	34	CK410 SRC CLKREQ8 L	
DOT96C/27MHZ_SPREAD	7	34	CK410 DOT96 27M N	(GMCH D_REFCLKIN DISPLAY PLL A 96MHZ)
DOT96T/27MHZ_NON-SPREAD	6	34	CK410 DOT96 27M P	
(INT PD) VTT_PWRGD*/PD	2	34	CK410 PD VTT_PWRGD L	(FROM CPU VCORE PWR GOOD)
FSA/48M	4	34	CK410 USB48 FSA	(ICH7M USB 48MHZ)
REF0/FSC	54	34	CK410 CLK14P3M_TIMER	(ICH7M, SIO, LPC REF. 14.318MHZ)
(INT PD) REF1/FCTSEL0	53	34	CK410 REF1_FCTSEL0	

FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11	
0	0	DOT96T	DOT96C	100MT_SST	100MC_SST	* FOR INT. GRAPHIC SYSTEM
0	1	DOT96T	DOT96C	SRCT0	SRCC0	
1	0	27M NON SPREAD	27M SPREAD	SRCT0	SRCC0	* FOR EXT. GRAPHIC SYSTEM
1	1	OFF LOW	TBD	SRCT0	SRCC0	

CLOCKS

SYNC_MASTER=MASTER SYNC_DATE=MASTER

NOTICE OF PROPRIETARY PROPERTY

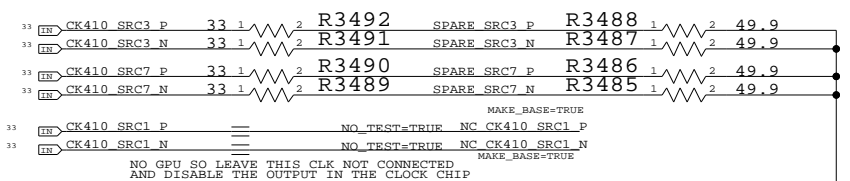
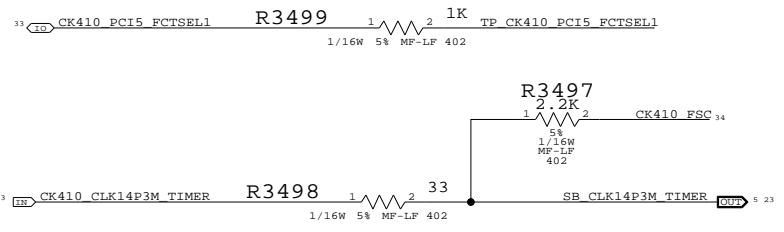
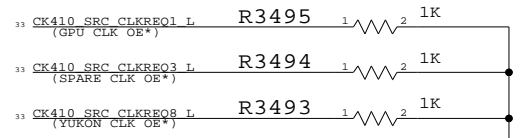
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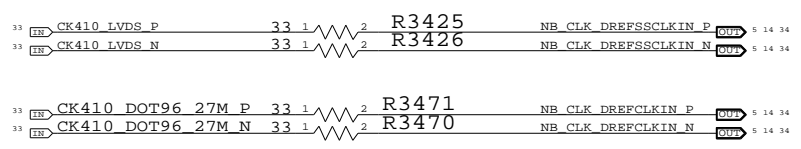
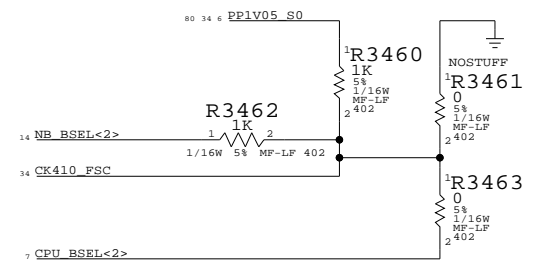
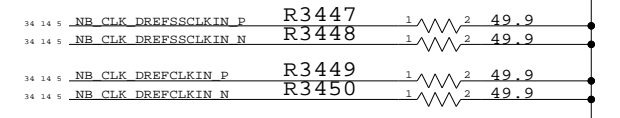
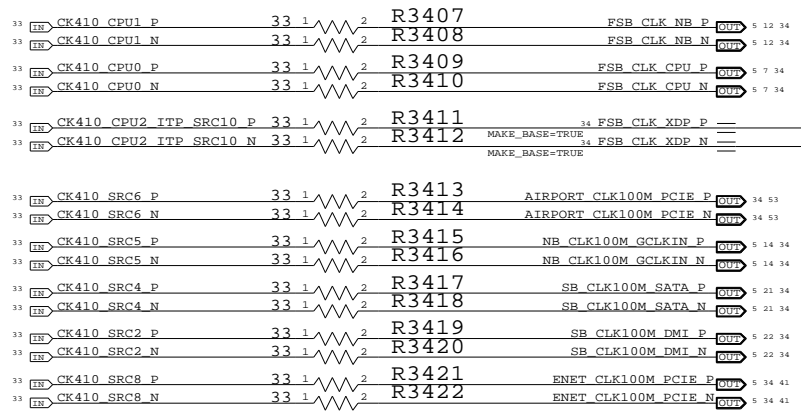
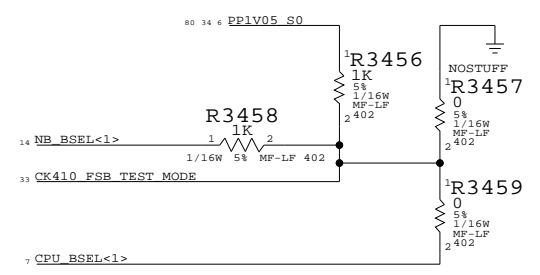
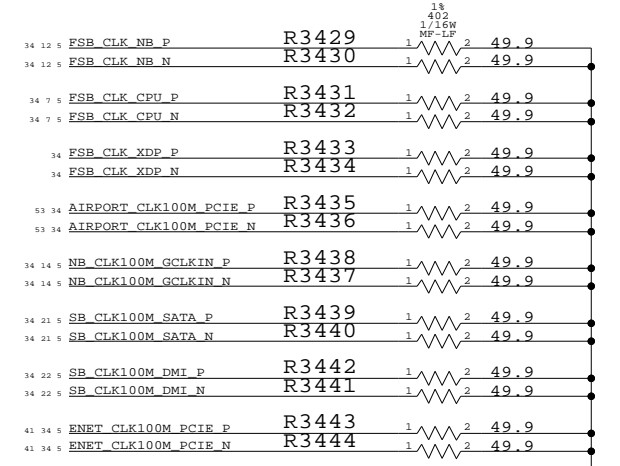
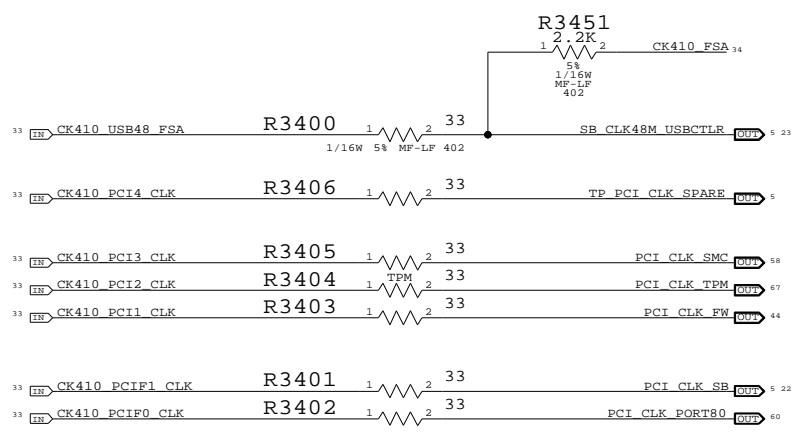
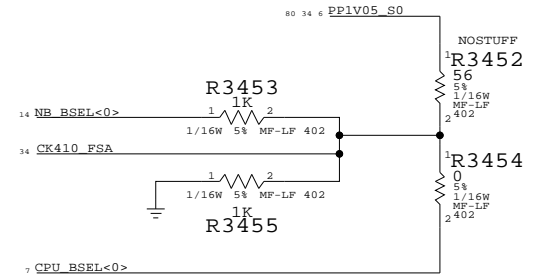
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NOTE: USE THESE PULL-DOWNS IF NOT CONNECTED TO GPIO'S



FSB FREQUENCY SELECT:

	STUFF	NO STUFF
CPU DRIVEN	R3453 R3454 R3455	R3456 R3457 R3458
533MHZ (133MHZ CPU CLK)	R3452 R3454 R3455	R3456 R3457 R3458
667MHZ (166MHZ CPU CLK)	R3452 R3454 R3455	R3456 R3457 R3458



CLOCKS: TERMINATIONS

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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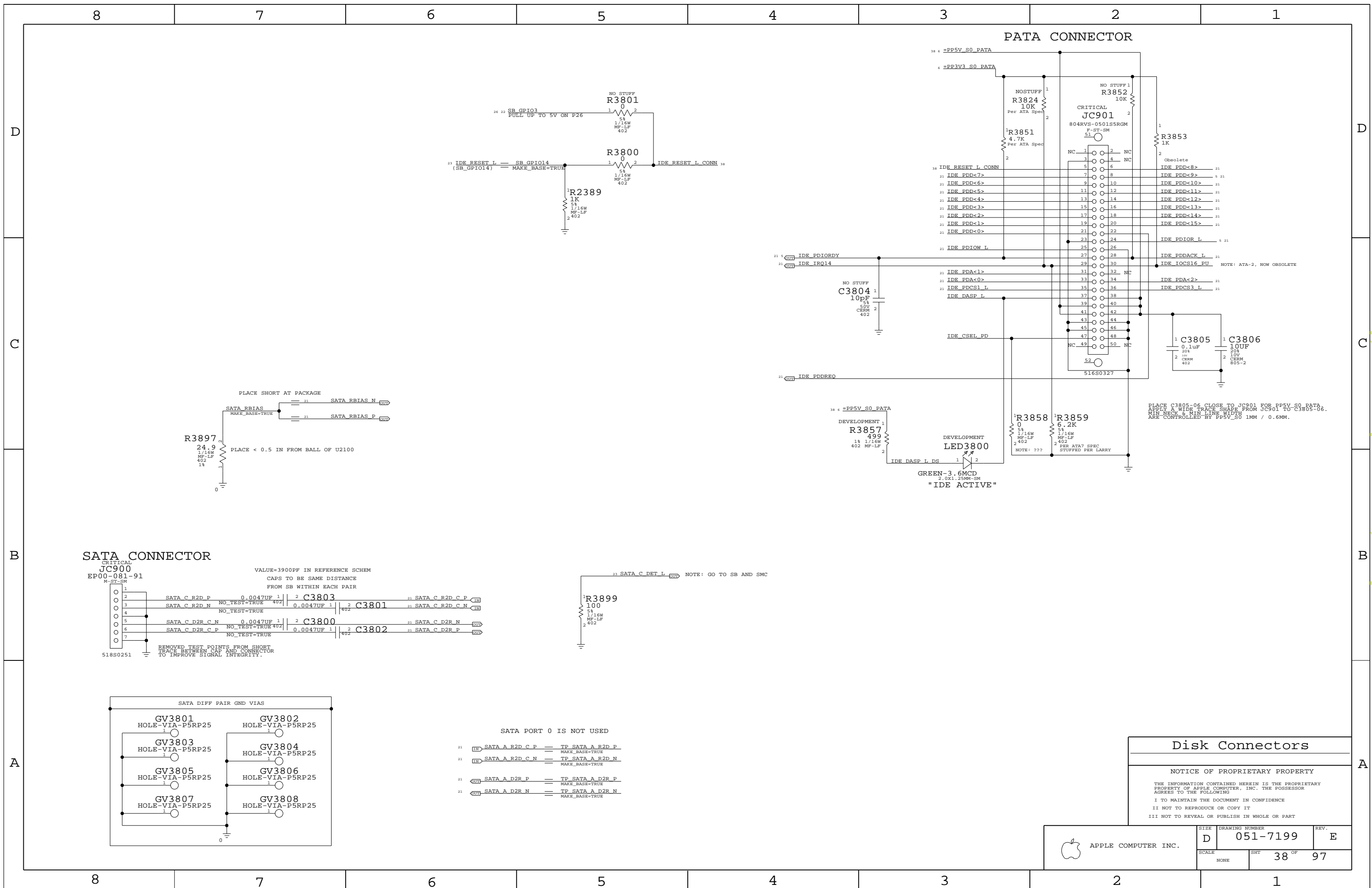
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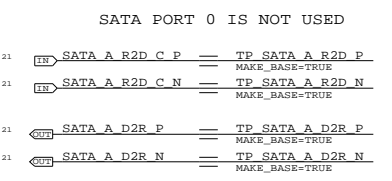
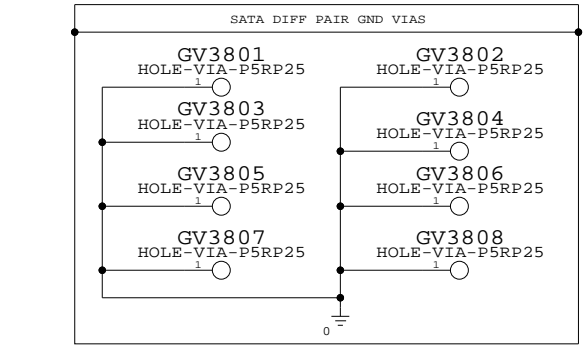
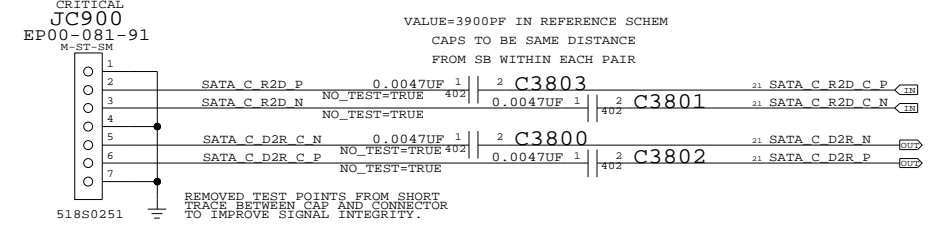
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	D	051-7199	E
SCALE	SHT	34 OF	97
NONE			

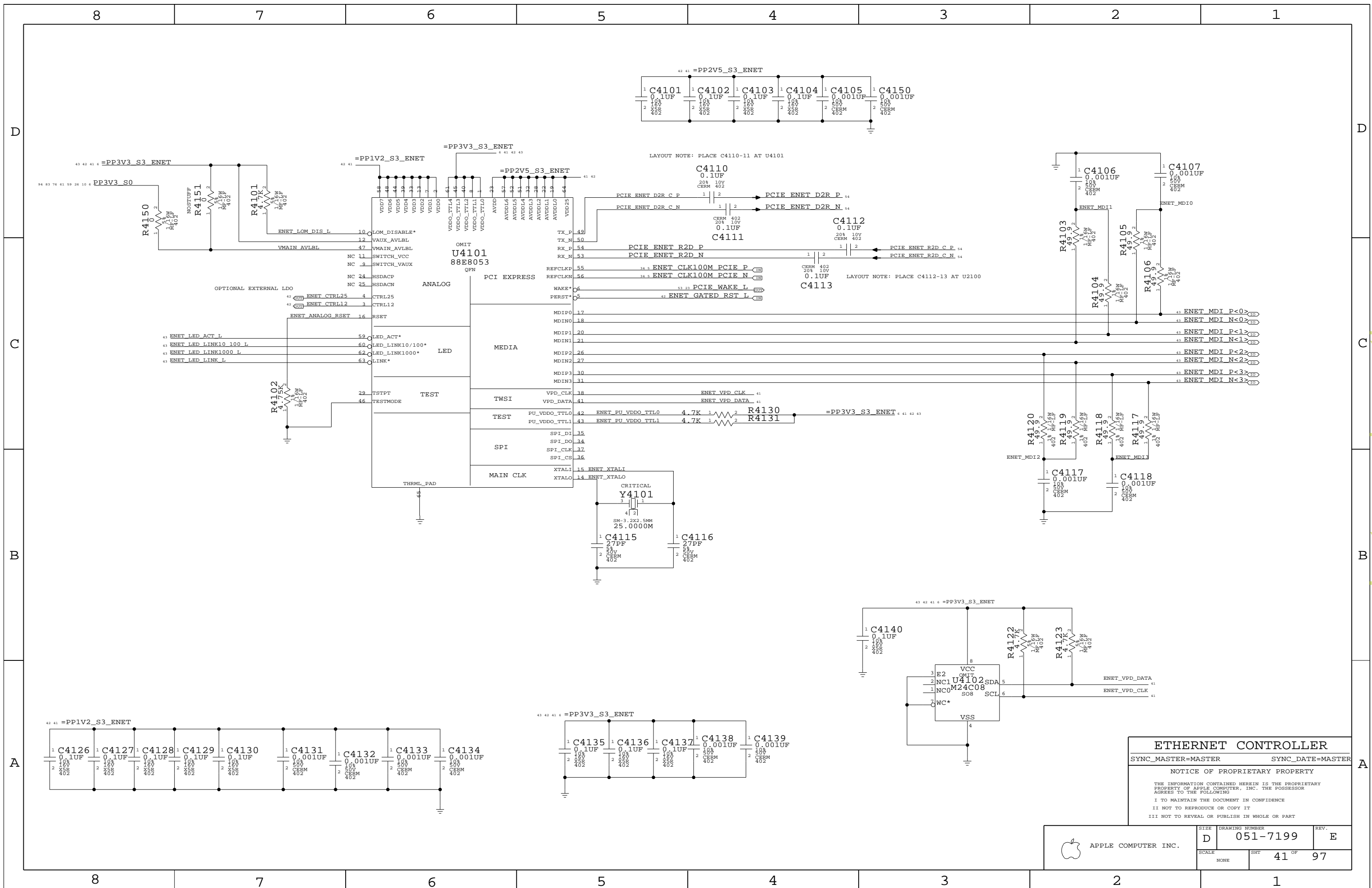


SATA CONNECTOR



Disk Connectors			
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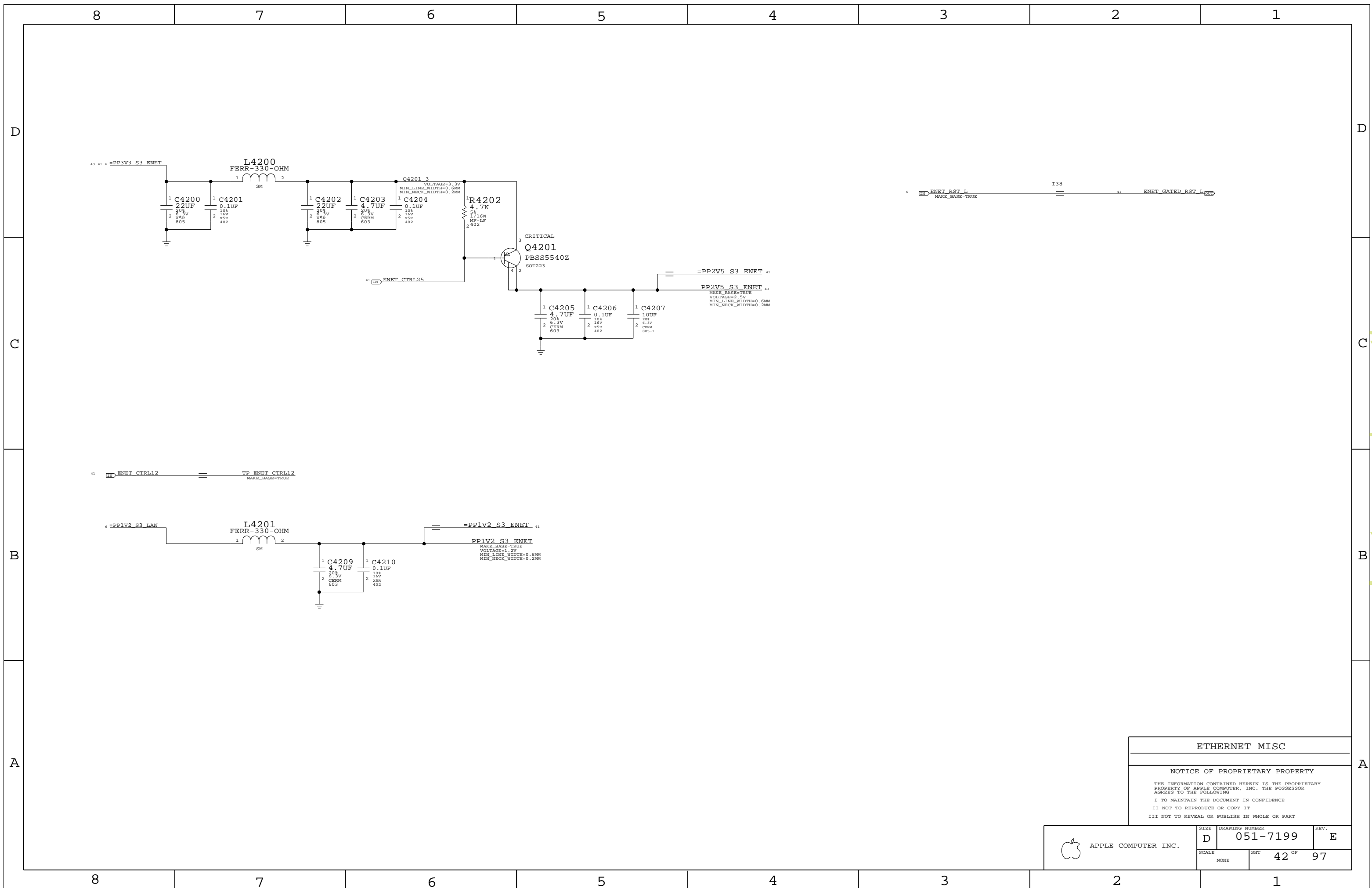
ETHERNET CONTROLLER

SYNC_MASTER=MASTER SYNC_DATA=MASTER

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	SCALE NONE	SHEET 41 OF 97	



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ETHERNET MISC

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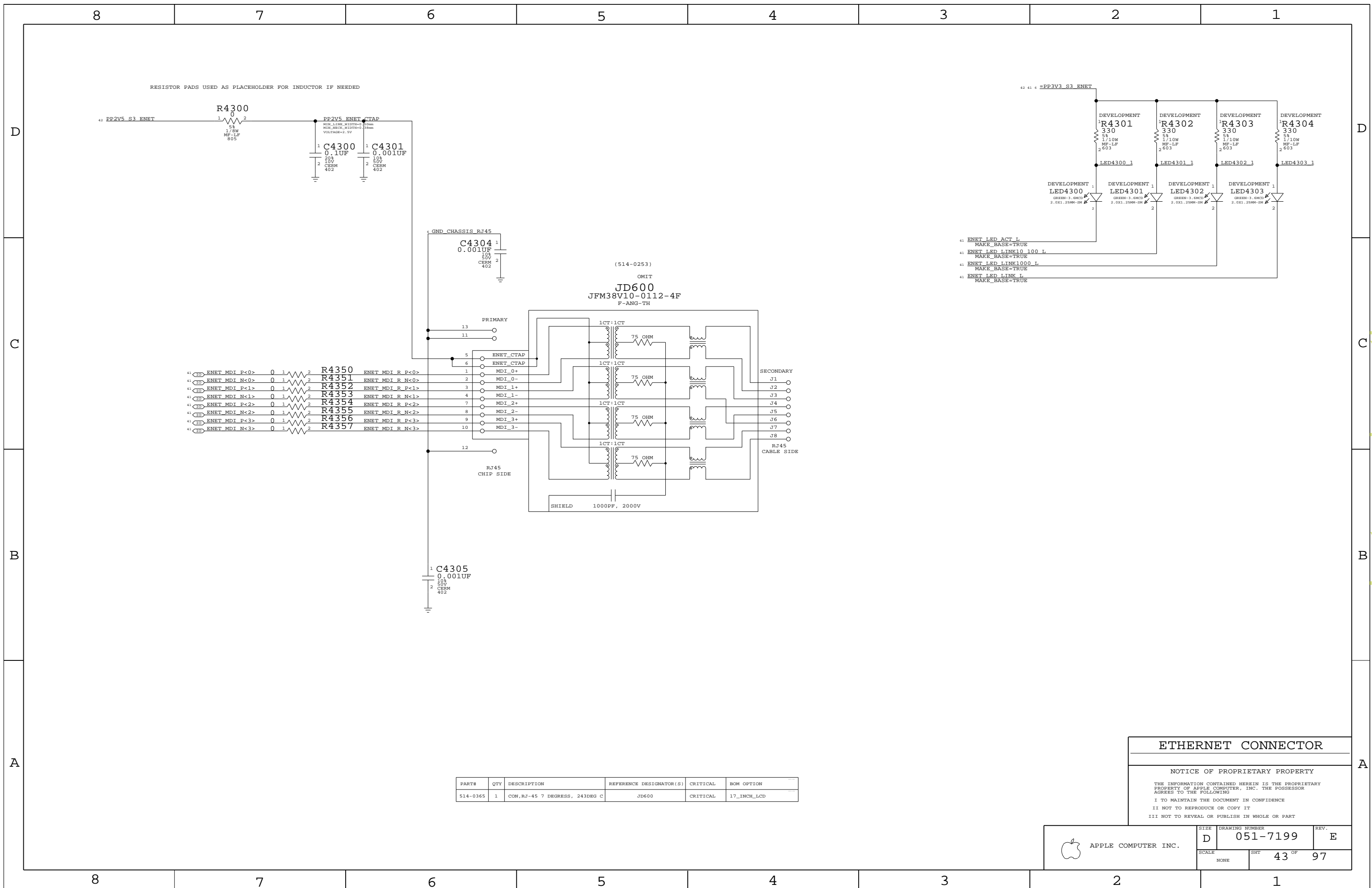
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7199	REV. E
	SCALE NONE	SHIT 42 OF 97	



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0365	1	CON,RJ-45 7 DEGRESS, 243DEG C	JD600	CRITICAL	17_INCH_LCD

ETHERNET CONNECTOR

NOTICE OF PROPRIETARY PROPERTY

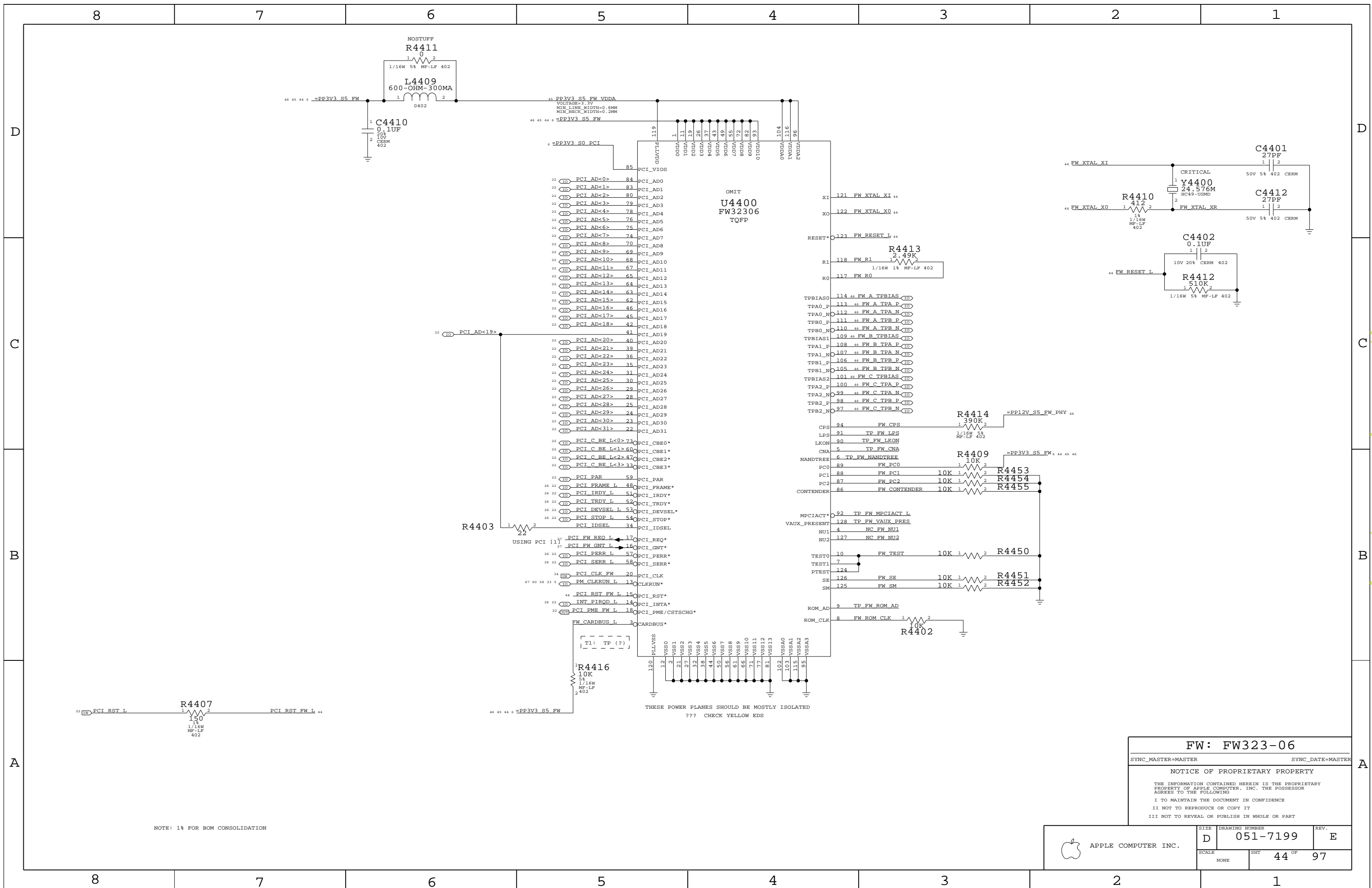
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	D	051-7199	E
SCALE	SHT	43 OF 97	
NONE			



NOTE: 1% FOR BOM CONSOLIDATION

FW: FW323-06

SYNC_MASTER=MASTER SYNC_DATE=MASTER

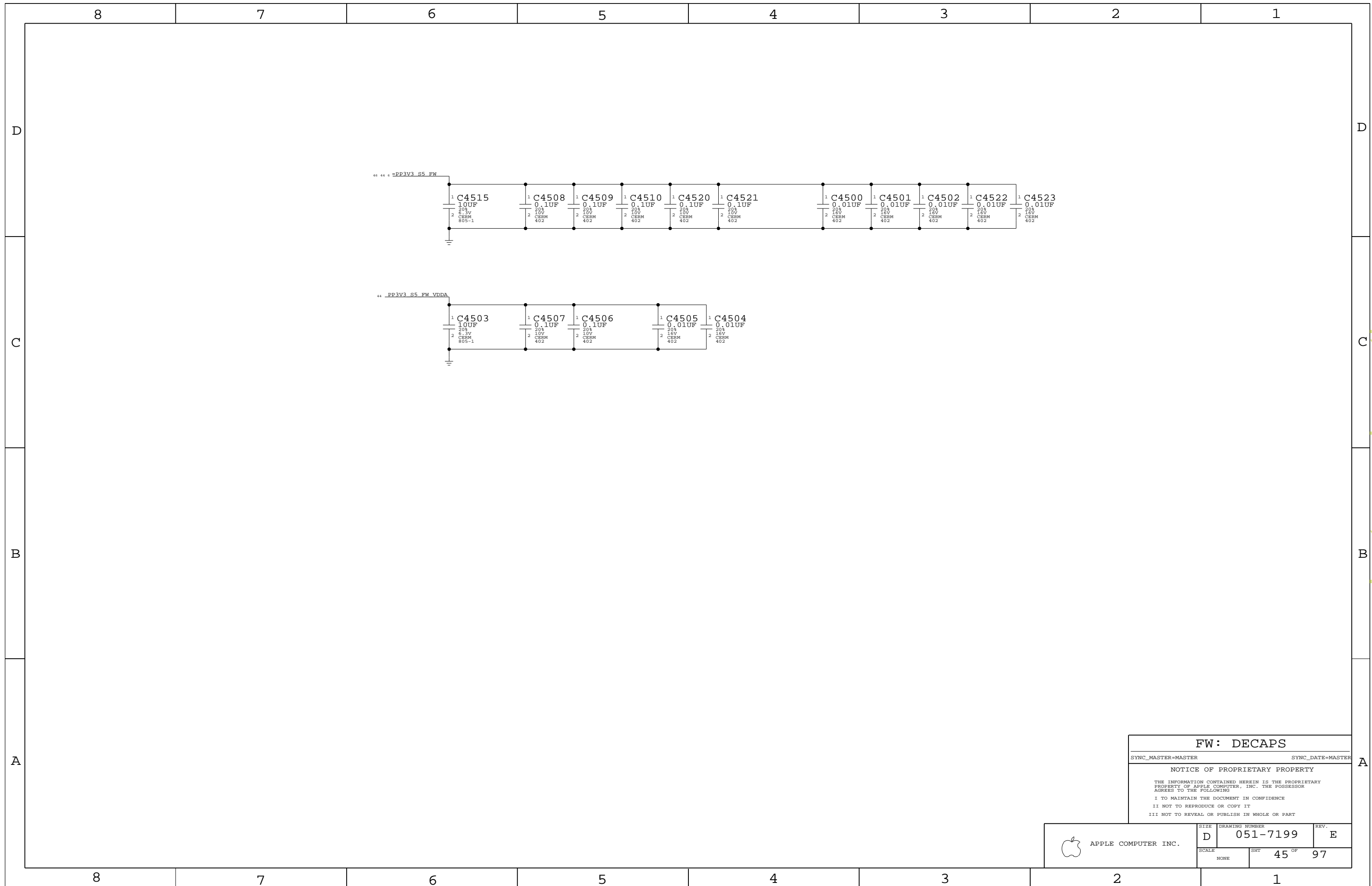
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	SCALE NONE	SHT 44 OF	97

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FW: DECAPS

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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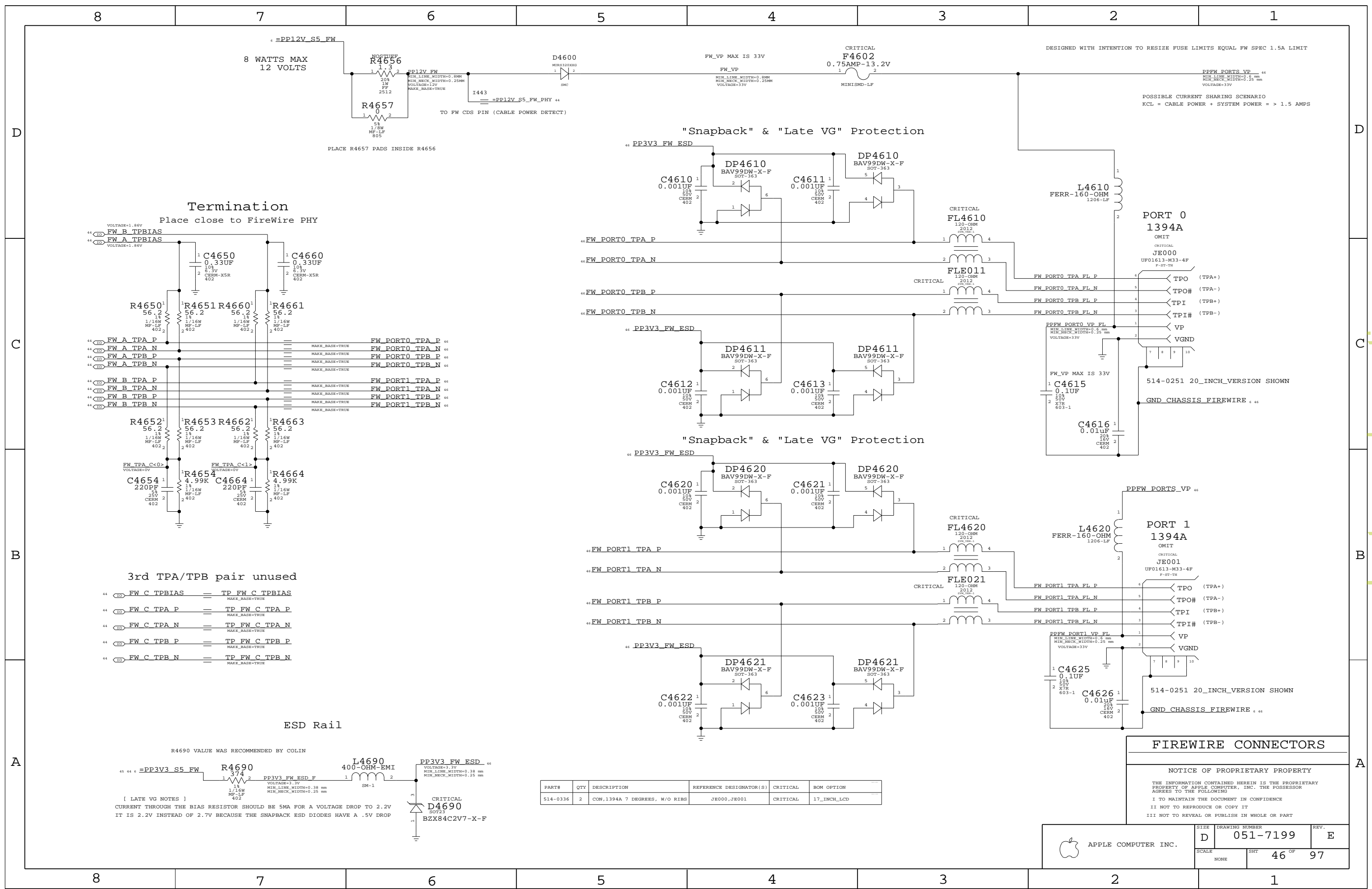
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7199	REV. E
	SCALE NONE	SHIT 45 OF 97	



Termination
Place close to FireWire PHY

"Snapback" & "Late VG" Protection

"Snapback" & "Late VG" Protection

3rd TPA/TPB pair unused

ESD Rail

FIREWIRE CONNECTORS

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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0336	2	CON,1394A 7 DEGREES, W/O RIBS	JE000,JE001	CRITICAL	17_INCH_LCD

APPLE COMPUTER INC.

SCALE: NONE

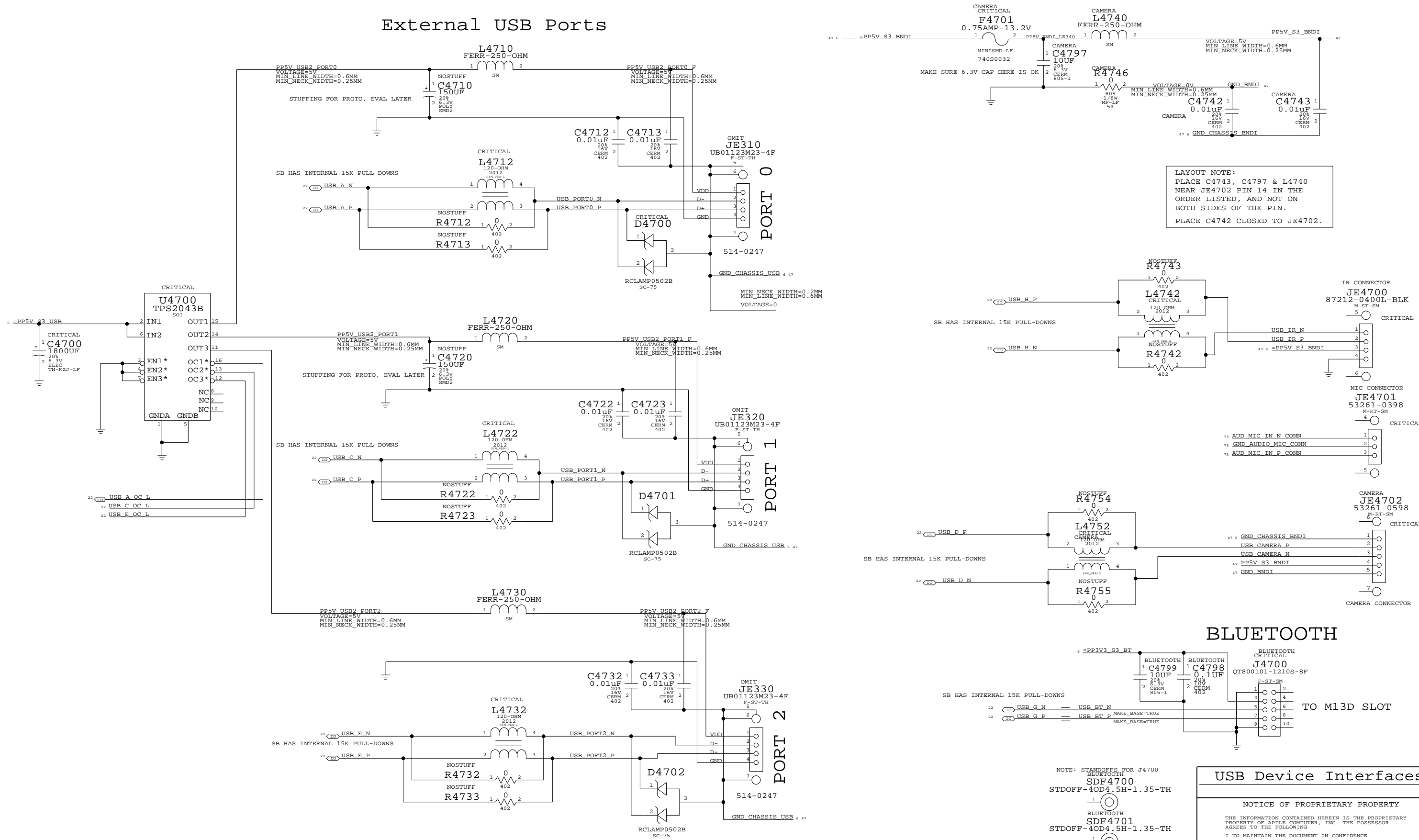
DRAWING NUMBER: 051-7199

SHT: 46 OF 97

REV: E

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External USB Ports



LAYOUT NOTE:
 PLACE C4743, C4797 & L4740
 NEAR JE4702 PIN 14 IN THE
 ORDER LISTED, AND NOT ON
 BOTH SIDES OF THE PIN.
 PLACE C4742 CLOSED TO JE4702.

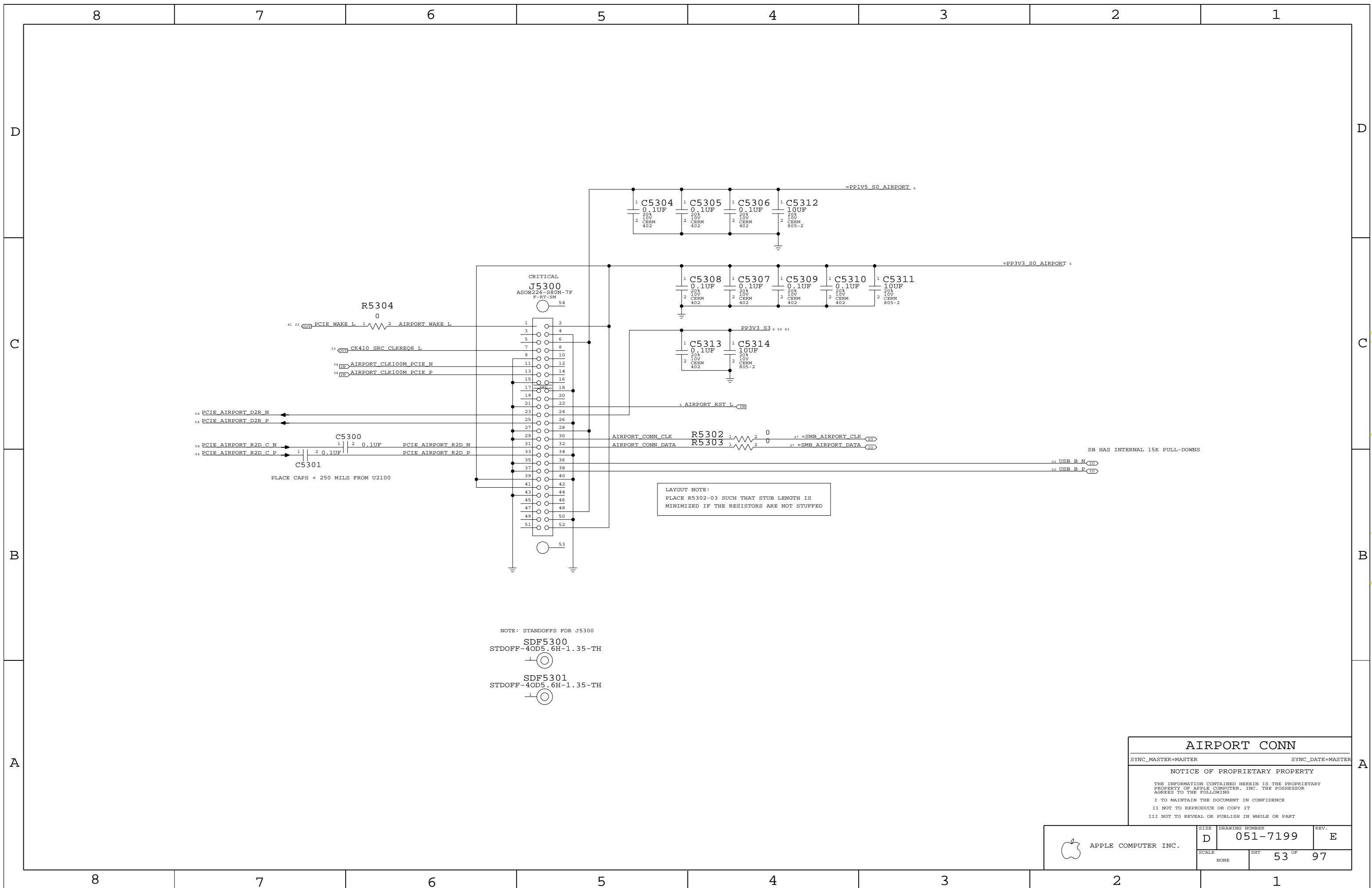
BLUETOOTH

USB Device Interfaces

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PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0339	3	USB RECEPTACLE, 4P, UB1123-M50-4F	JE310, JE320, JE330	CRITICAL	17_INCH_LCD

APPLE COMPUTER INC.	SIZE	D	DRAWING NUMBER	051-7199	REV.	E
	SCALE	NONE	SHT	47 OF 97		



R5304
0

41 23 PCIE WAKE L 1 2 AIRPORT WAKE L

33 CK410_SRC_CLKREQ6 L

34 AIRPORT_CLK100M_PCIE N

34 AIRPORT_CLK100M_PCIE P

54 PCIE_AIRPORT_D2R_N

54 PCIE_AIRPORT_D2R_P

54 PCIE_AIRPORT_R2D_C_N

54 PCIE_AIRPORT_R2D_C_P

C5300
1 2 0.1UF
PCIE_AIRPORT_R2D_N
PCIE_AIRPORT_R2D_P

C5301

PLACE CAPS < 250 MILS FROM U2100

AIRPORT_CONN_CLK R5302 1 2 0
AIRPORT_CONN_DATA R5303 1 2 0

PP3V3_S3 6 59 83

C5308 0.1UF 20% 10V CERAM 402
C5307 0.1UF 20% 10V CERAM 402
C5309 0.1UF 20% 10V CERAM 402
C5310 0.1UF 20% 10V CERAM 402
C5311 10UF 20% 10V CERAM 805-2

C5313 0.1UF 20% 10V CERAM 402
C5314 10UF 20% 10V CERAM 805-2

LAYOUT NOTE:
PLACE R5302-03 SUCH THAT STUB LENGTH IS
MINIMIZED IF THE RESISTORS ARE NOT STUFFED

SB HAS INTERNAL 15K PULL-DOWNS

22 USB_B_N

22 USB_B_P

NOTE: STANDOFFS FOR J5300

SDF5300
STDOFF-40D5.6H-1.35-TH



SDF5301
STDOFF-40D5.6H-1.35-TH



AIRPORT CONN

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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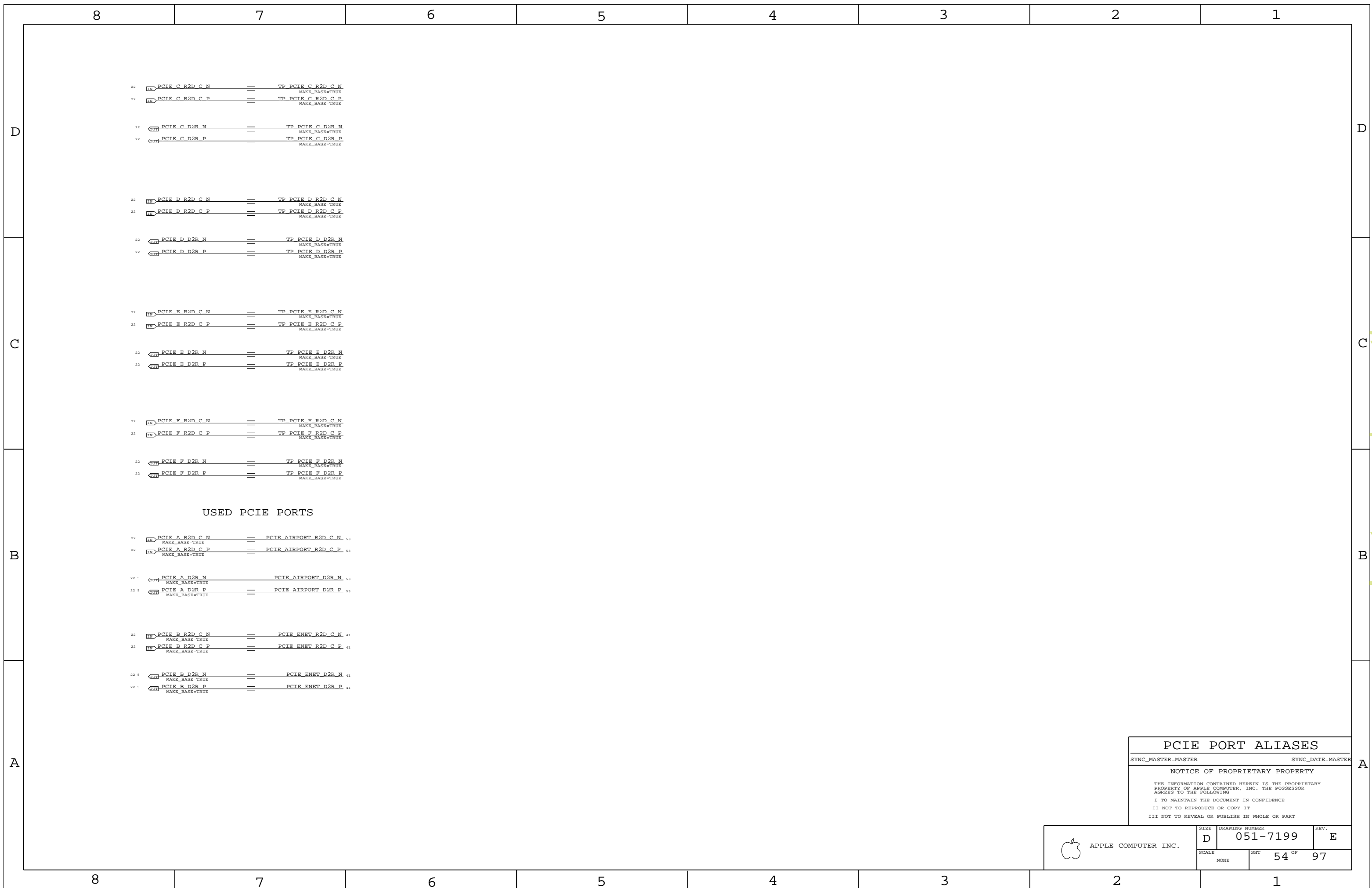
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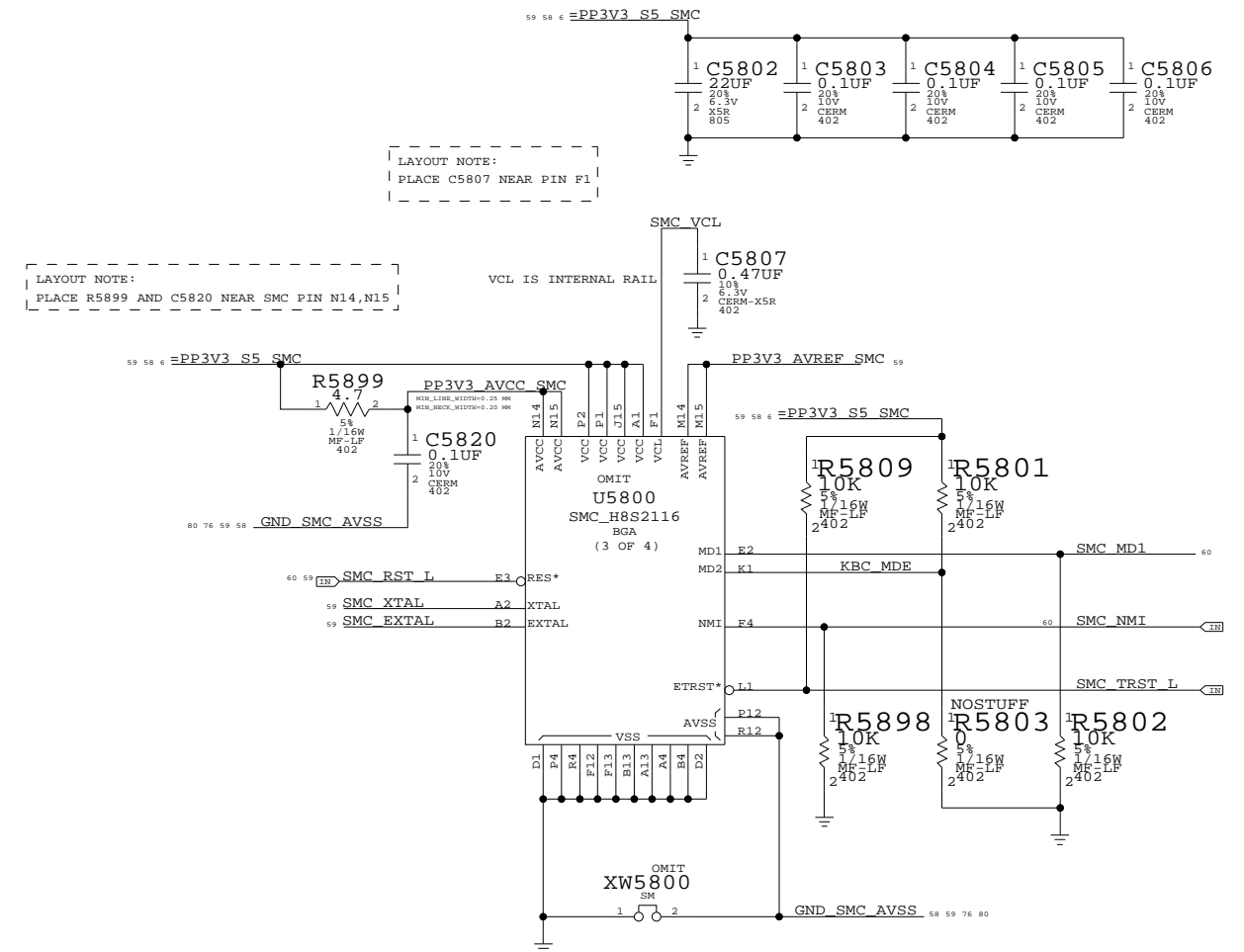
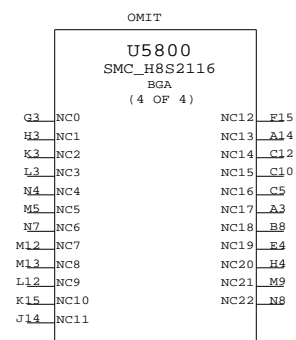
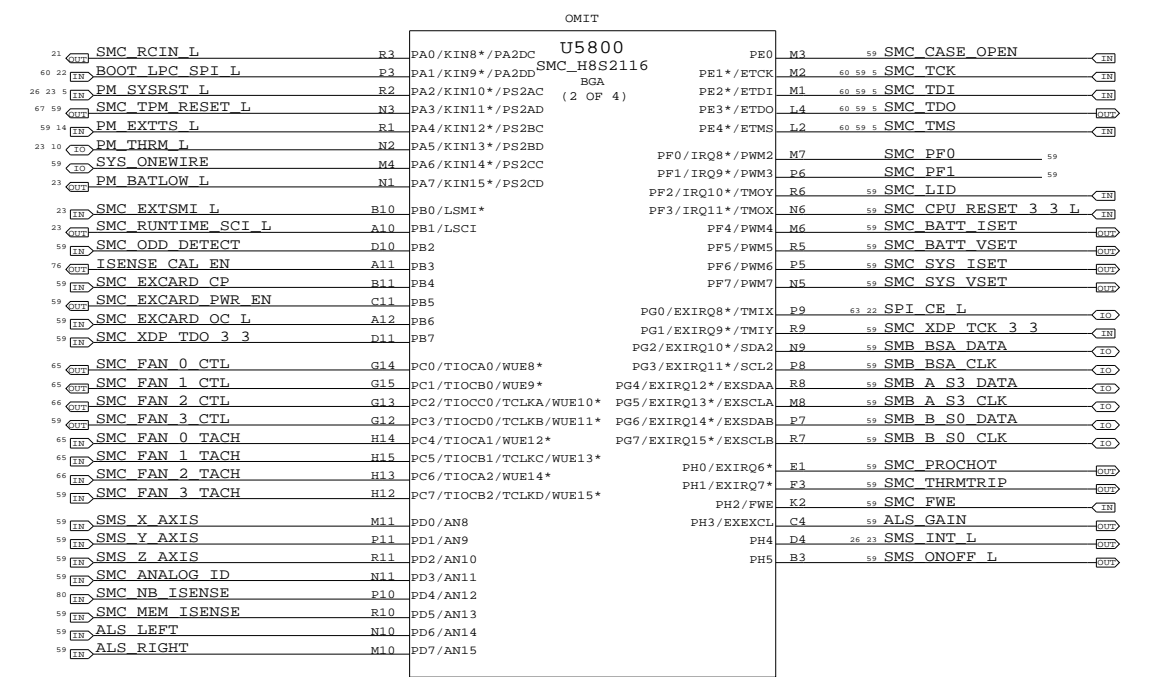
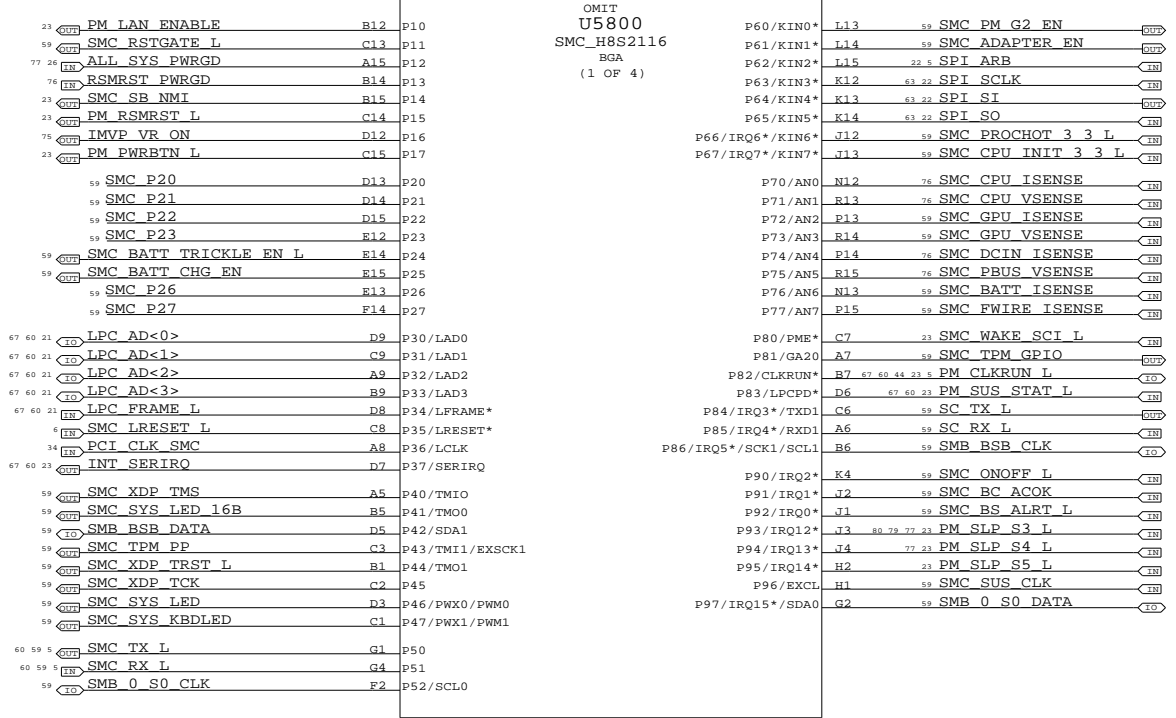
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	D	051-7199	E
SCALE	SHT	53 OF 97	
NONE			



PCIE PORT ALIASES
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	SCALE	SHT	OF
	NONE	54	97

UNUSED PINS HAVE THE FORMAT SMC_XXX WHERE XXX IS THE PORT NUMBER. THEY ARE SET BY SOFTWARE TO BE DRIVEN OUTPUTS ALWAYS SO THEY CAN BE LEFT NO-CONNECTED.



LAYOUT NOTE:
PLACE C5807 NEAR PIN F1

LAYOUT NOTE:
PLACE R5899 AND C5820 NEAR SMC PIN N14,N15

SMC

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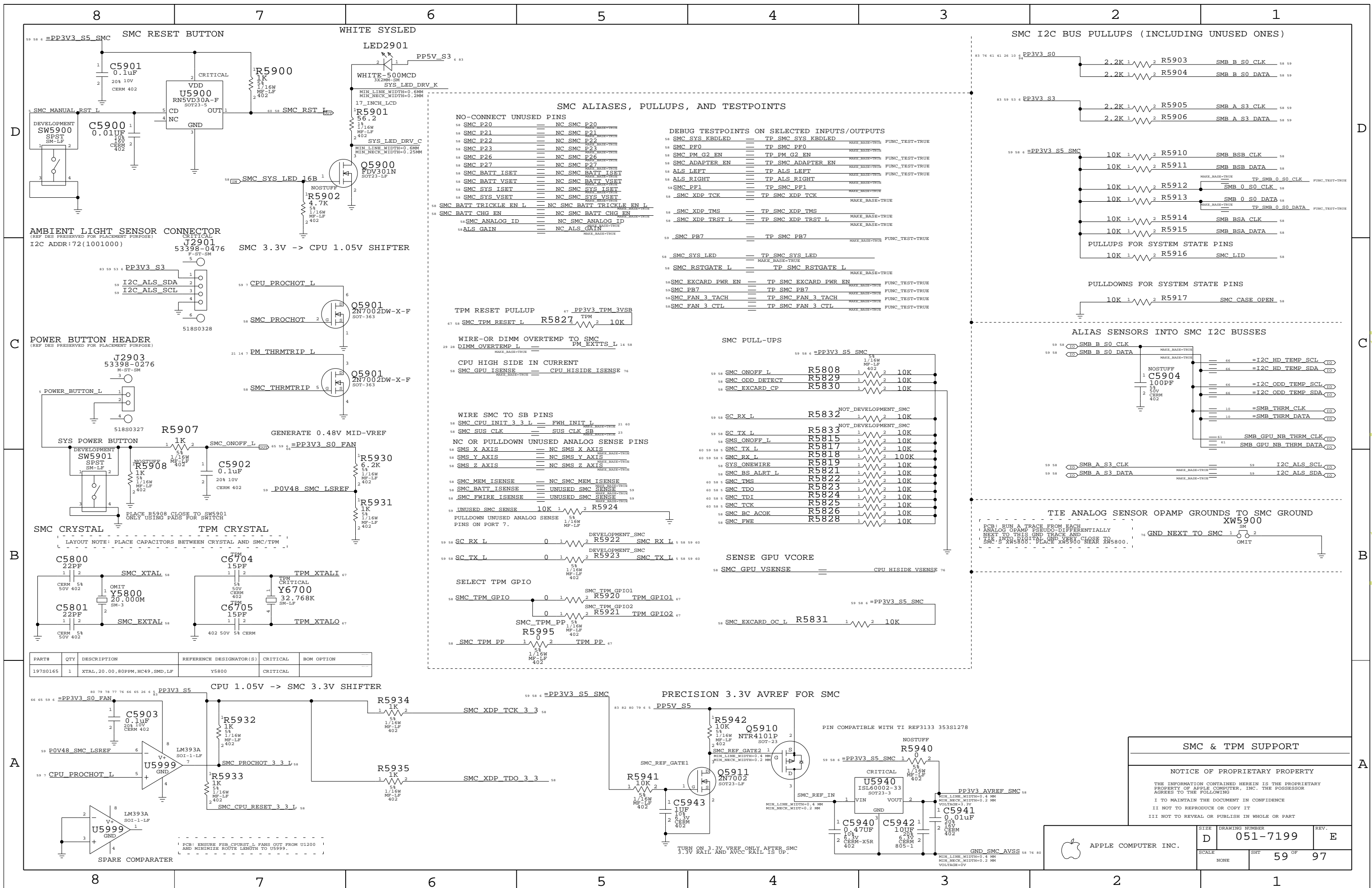
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SCALE	SHT	58 OF	97
NONE			

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SMC ALIASES, PULLUPS, AND TESTPOINTS

NO-CONNECT UNUSED PINS	DEBUG TESTPOINTS ON SELECTED INPUTS/OUTPUTS
SMC P20 = NC SMC P20	SMC SYS_KBDLED = TP_SMC_SYS_KBDLED
SMC P21 = NC SMC P21	SMC PF0 = TP_SMC_PF0
SMC P22 = NC SMC P22	SMC PM_G2_EN = TP_PM_G2_EN
SMC P23 = NC SMC P23	SMC_ADAPTER_EN = TP_SMC_ADAPTER_EN
SMC P26 = NC SMC P26	ALS_LEFT = TP_ALS_LEFT
SMC P27 = NC SMC P27	ALS_RIGHT = TP_ALS_RIGHT
SMC_BATT_ISET = NC SMC_BATT_ISET	SMC_PFI = TP_SMC_PFI
SMC_BATT_VSET = NC SMC_BATT_VSET	SMC_XDP_TCK = TP_SMC_XDP_TCK
SMC_SYS_ISET = NC SMC_SYS_ISET	SMC_XDP_TMS = TP_SMC_XDP_TMS
SMC_SYS_VSET = NC SMC_SYS_VSET	SMC_XDP_TRST_L = TP_SMC_XDP_TRST_L
SMC_BATT_TRICKLE_EN_L = NC SMC_BATT_TRICKLE_EN_L	SMC_PB7 = TP_SMC_PB7
SMC_BATT_CHG_EN = NC SMC_BATT_CHG_EN	SMC_SYS_LED = TP_SMC_SYS_LED
SMC_ANALOG_ID = NC SMC_ANALOG_ID	SMC_RSTGATE_L = TP_SMC_RSTGATE_L
ALS_GAIN = NC ALS_GAIN	SMC_EXCARD_PWR_EN = TP_SMC_EXCARD_PWR_EN
	SMC_PB7 = TP_SMC_PB7
	SMC_FAN_3_TACH = TP_SMC_FAN_3_TACH
	SMC_FAN_3_CTL = TP_SMC_FAN_3_CTL

SMC PULL-UPS

SMC_ONOFF_L	R5808	10K
SMC_ODD_DETECT	R5829	10K
SMC_EXCARD_CP	R5830	10K
SC_RX_L	R5832	10K
SC_TX_L	R5833	10K
SMS_ONOFF_L	R5815	10K
SMC_TX_L	R5817	10K
SMC_RX_L	R5818	100K
SYS_ONEWIRE	R5819	10K
SMC_BS_ALERT_L	R5821	10K
SMC_TMS	R5822	10K
SMC_TDO	R5823	10K
SMC_TDI	R5824	10K
SMC_TCK	R5825	10K
SMC_BC_ACOK	R5826	10K
SMC_FWE	R5828	10K

WIRE SMC TO SB PINS

SMC_CPU_INIT_3_3_L	FWH_INIT_L
SMC_SUS_CLK	SUS_CLK_SB
SMS_X_AXIS	NC_SMS_X_AXIS
SMS_Y_AXIS	NC_SMS_Y_AXIS
SMS_Z_AXIS	NC_SMS_Z_AXIS
SMC_MEM_ISENSE	NC_SMC_MEM_ISENSE
SMC_BATT_ISENSE	UNUSED_SMC_ISENSE
SMC_FWIRE_ISENSE	UNUSED_SMC_ISENSE
UNUSED_SMC_SENSE	10K
PULLDOWN_UNUSED_ANALOG_SENSE	5K

SELECT TPM GPIO

SMC_TPM_GPIO1	R5920	TPM_GPIO1
SMC_TPM_GPIO2	R5921	TPM_GPIO2
SMC_TPM_PP	R5995	TPM_PP
SMC_EXCARD_OC_L	R5831	10K

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0165	1	XTAL, 20.00, 80PPM, HC49, SMD, LF	Y5800	CRITICAL	

SMC & TPM SUPPORT

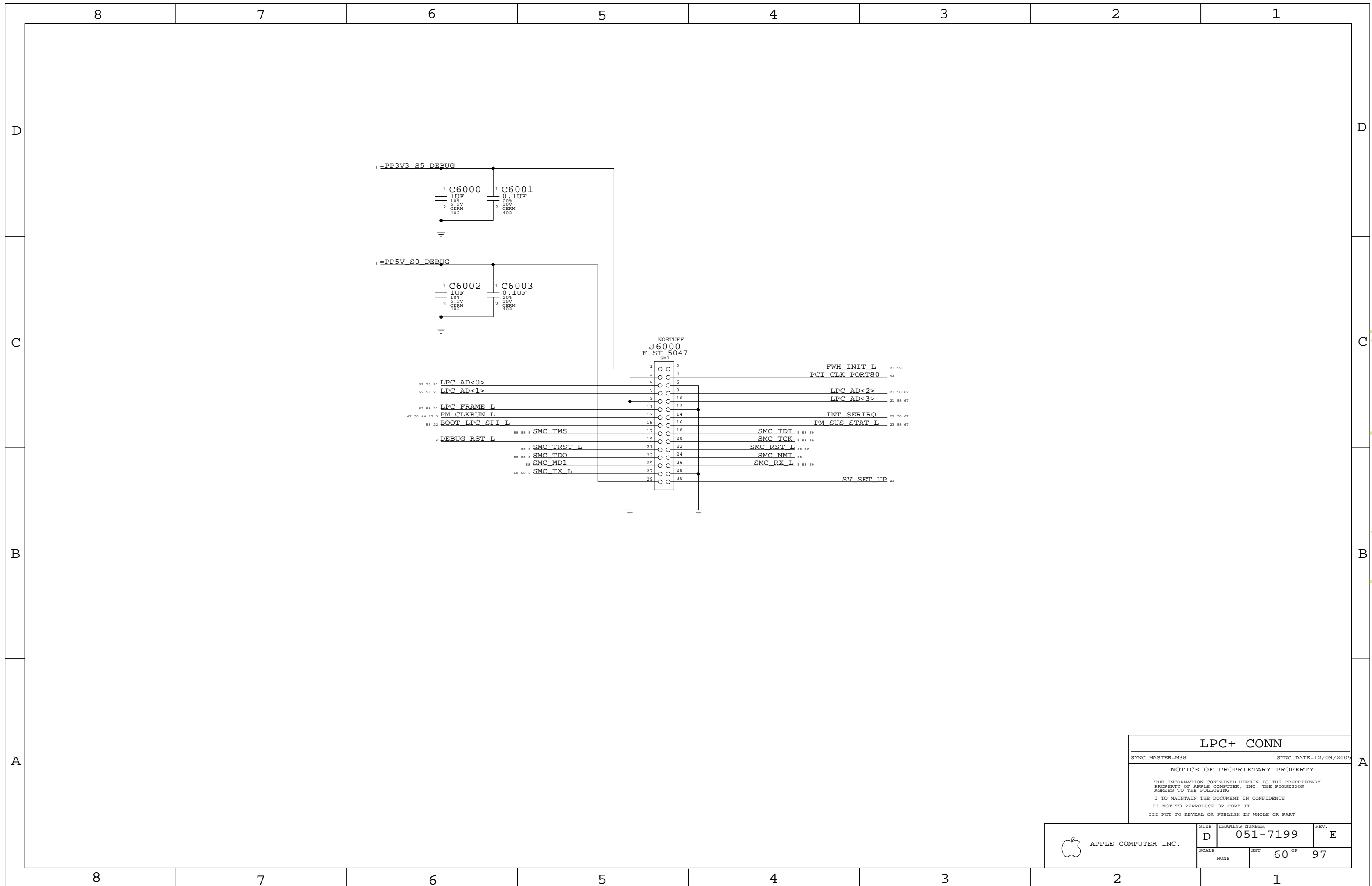
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SCALE	SHEET	59 OF 97	
NONE			

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LPC+ CONN

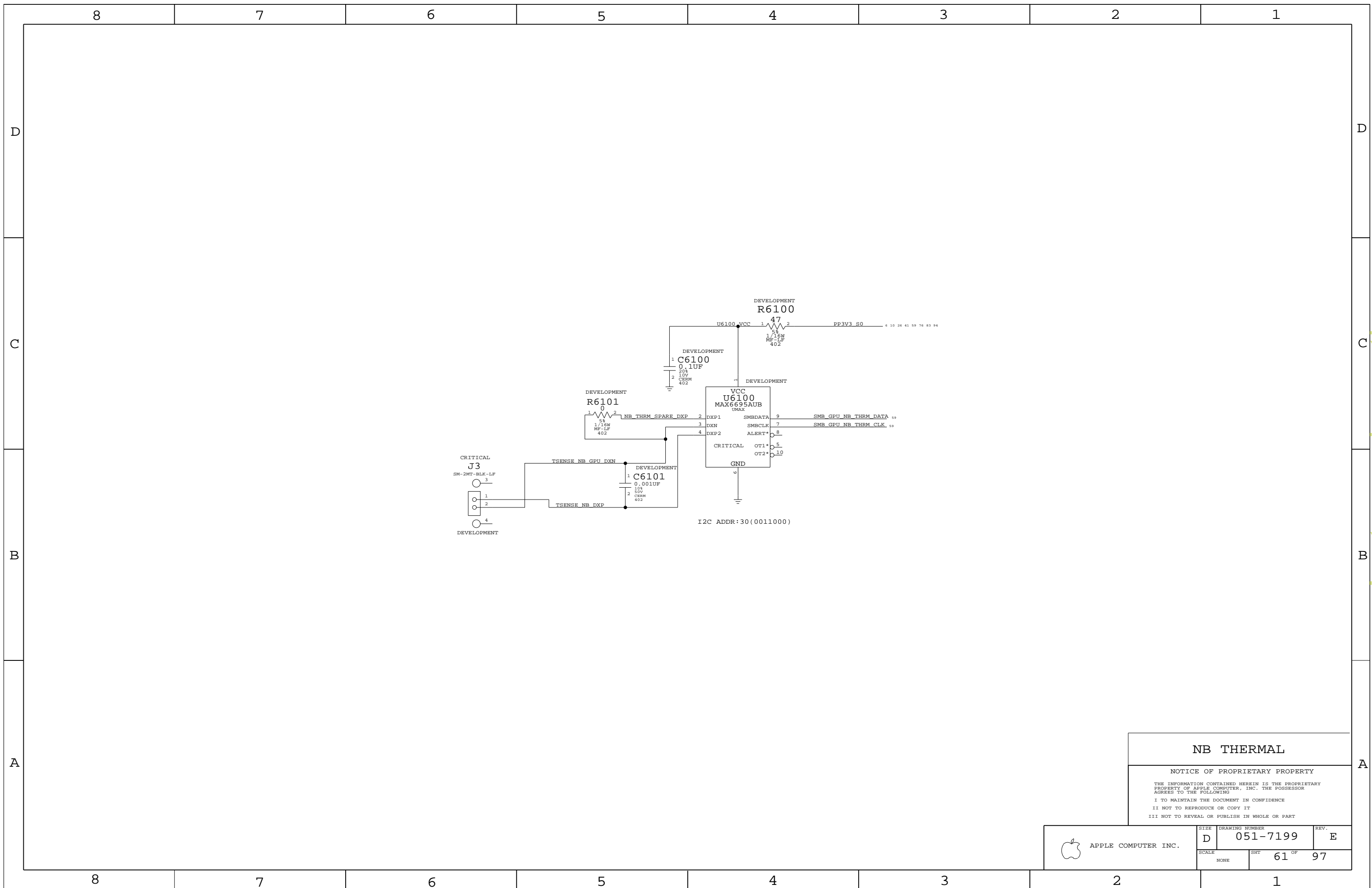
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SCALE	SHT	60 OF 97	
NONE			



NB THERMAL


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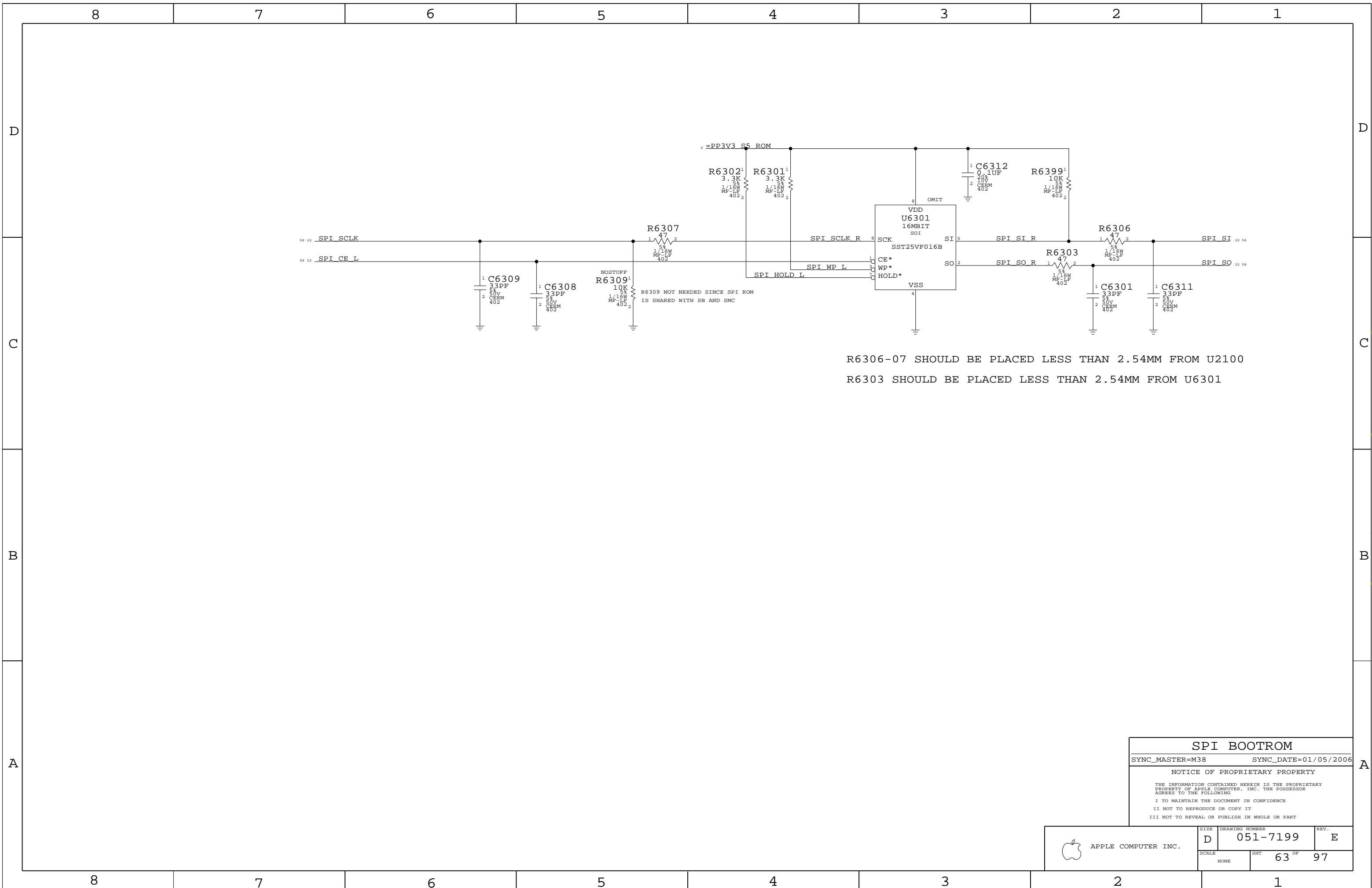
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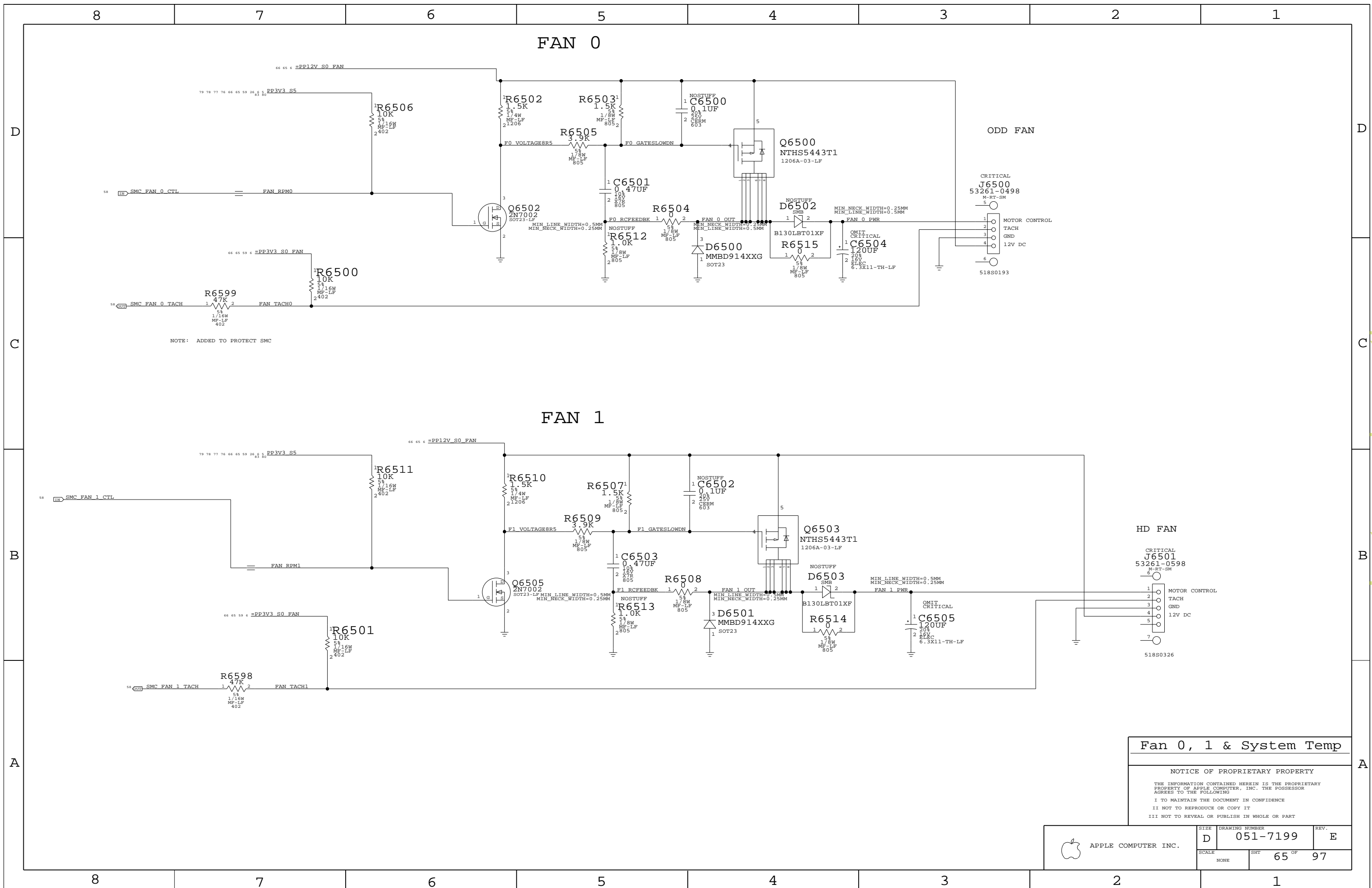
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	D	051-7199	E
SCALE	SHT	OF	
NONE	61	97	



R6306-07 SHOULD BE PLACED LESS THAN 2.54MM FROM U2100
 R6303 SHOULD BE PLACED LESS THAN 2.54MM FROM U6301

SPI BOOTROM
 SYNC_MASTER=M38 SYNC_DATE=01/05/2006
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7199	REV. E
	SCALE NONE	SHEET 63 OF 97	



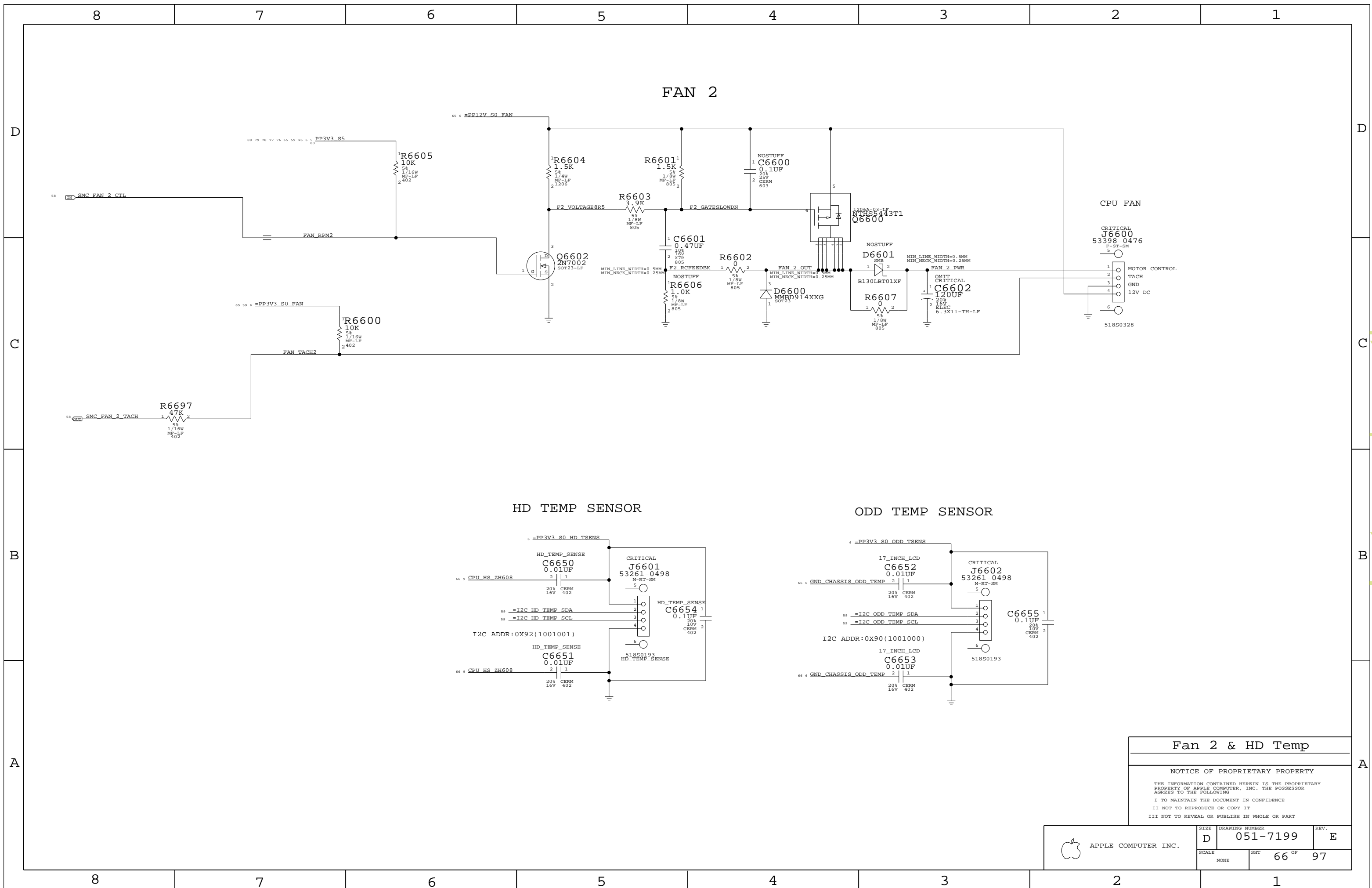
NOTE: ADDED TO PROTECT SMC

Fan 0, 1 & System Temp

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7199	REV. E
	SCALE NONE	SHEET 65 OF 97	



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Fan 2 & HD Temp

NOTICE OF PROPRIETARY PROPERTY

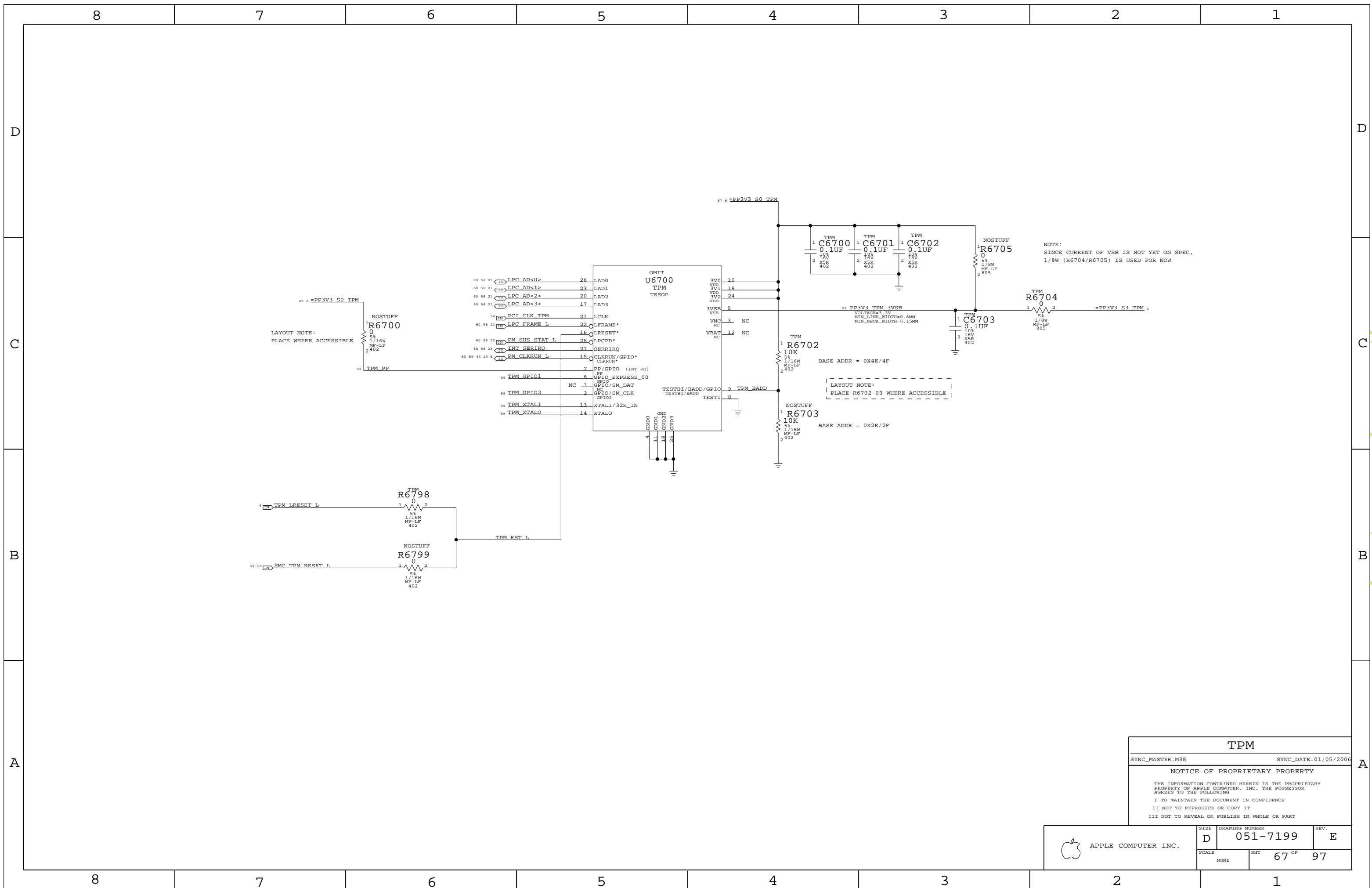
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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7199	REV. E
	SCALE NONE	SHEETS 66 OF 97	



LAYOUT NOTE:
PLACE WHERE ACCESSIBLE

LAYOUT NOTE:
PLACE R6702-03 WHERE ACCESSIBLE

NOTE:
SINCE CURRENT OF VSB IS NOT YET ON SPEC,
1/8W (R6704/R6705) IS USED FOR NOW

TPM

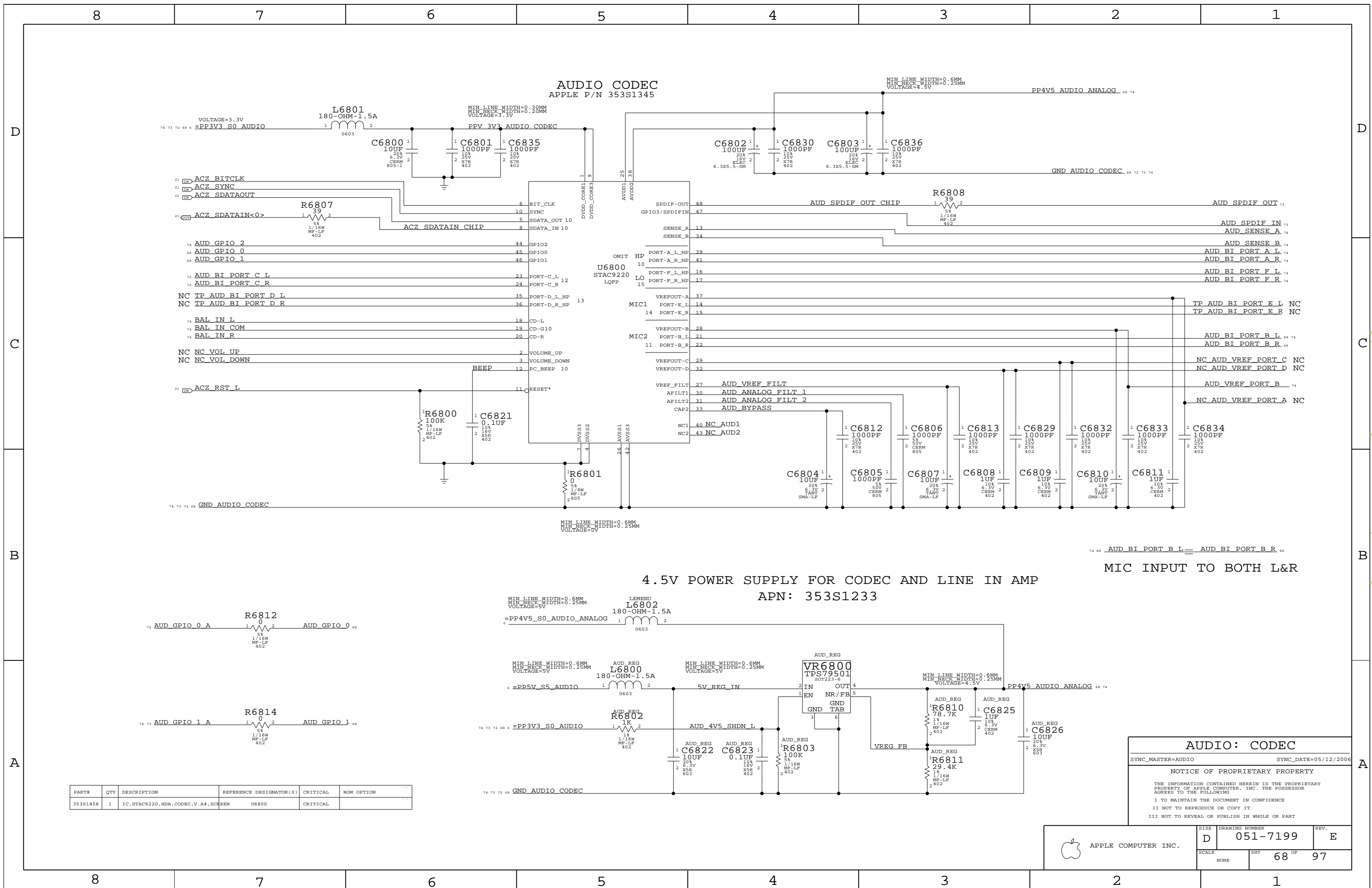
SYNC_MASTER=M38 SYNC_DATE=01/05/2006

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	SCALE NONE	SHT 67 OF 97	

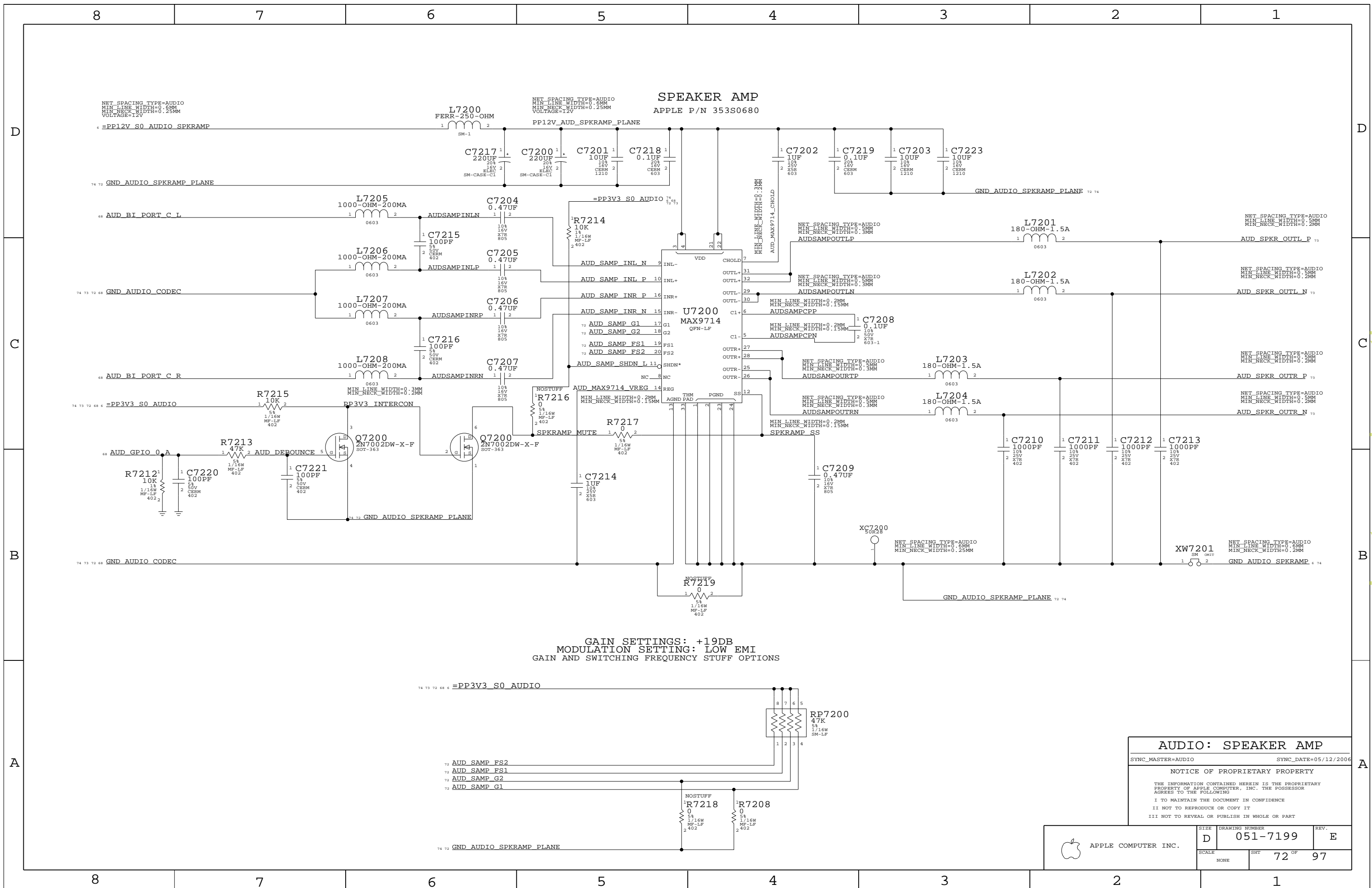


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S1458	1	IC, STAC9220, HDA, CODEC, V.A4, SCREEN	U6800	CRITICAL	

AUDIO: CODEC
 SYNC_MASTER=AUDIO SYNC_DATE=05/12/2006
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	SCALE NONE	SHEET 68 OF 97	

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GAIN SETTINGS: +19DB
 MODULATION SETTING: LOW EMI
 GAIN AND SWITCHING FREQUENCY STUFF OPTIONS

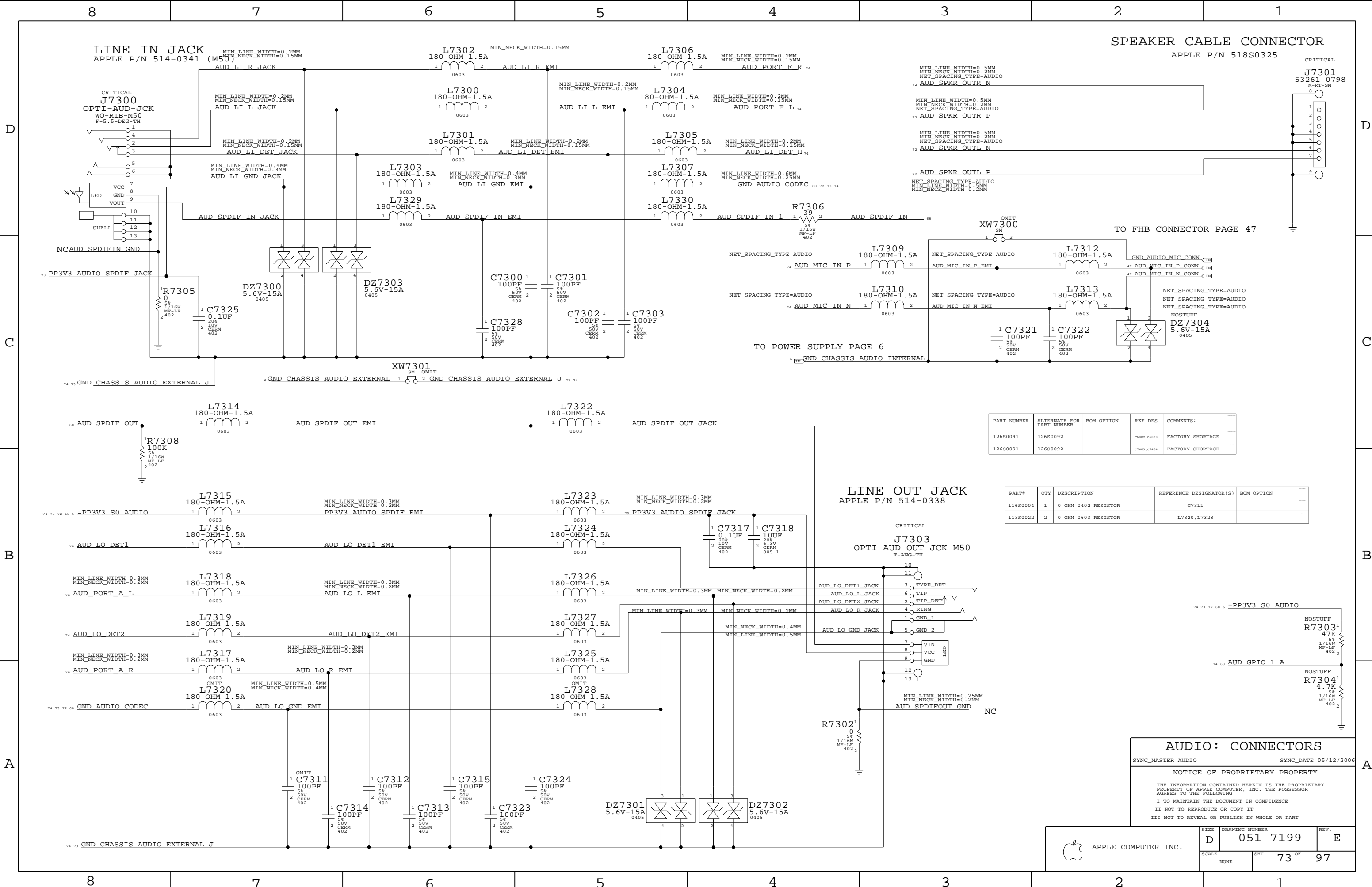
AUDIO: SPEAKER AMP
 SYNC_MASTER=AUDIO SYNC_DATE=05/12/2006
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	E
SCALE	SHT		72 OF 97
NONE			

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LINE IN JACK
APPLE P/N 514-0341 (M50)

SPEAKER CABLE CONNECTOR
APPLE P/N 518S0325



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
126S0091	126S0092		C802, C803	FACTORY SHORTAGE
126S0091	126S0092		C743, C744	FACTORY SHORTAGE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S0004	1	0 OHM 0402 RESISTOR	C7311	
113S0022	2	0 OHM 0603 RESISTOR	L7320, L7328	

LINE OUT JACK
APPLE P/N 514-0338

AUDIO: CONNECTORS

SYNC_MASTER=AUDIO SYNC_DATE=05/12/2006

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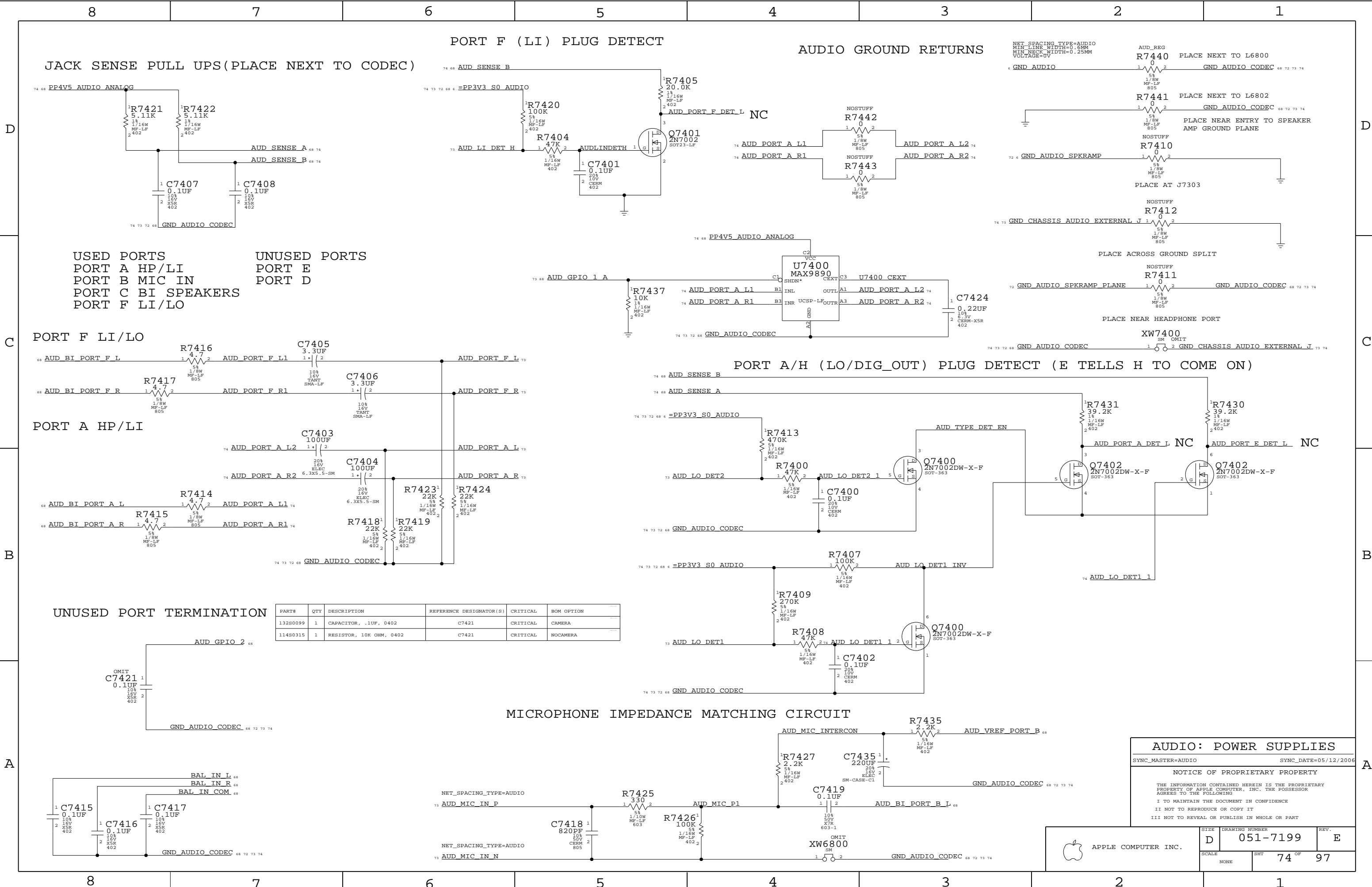
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	D	051-7199	E
SCALE	NONE	SHT	73 OF 97

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USED PORTS
 PORT A HP/LI
 PORT B MIC IN
 PORT C BI SPEAKERS
 PORT F LI/LO

UNUSED PORTS
 PORT E
 PORT D

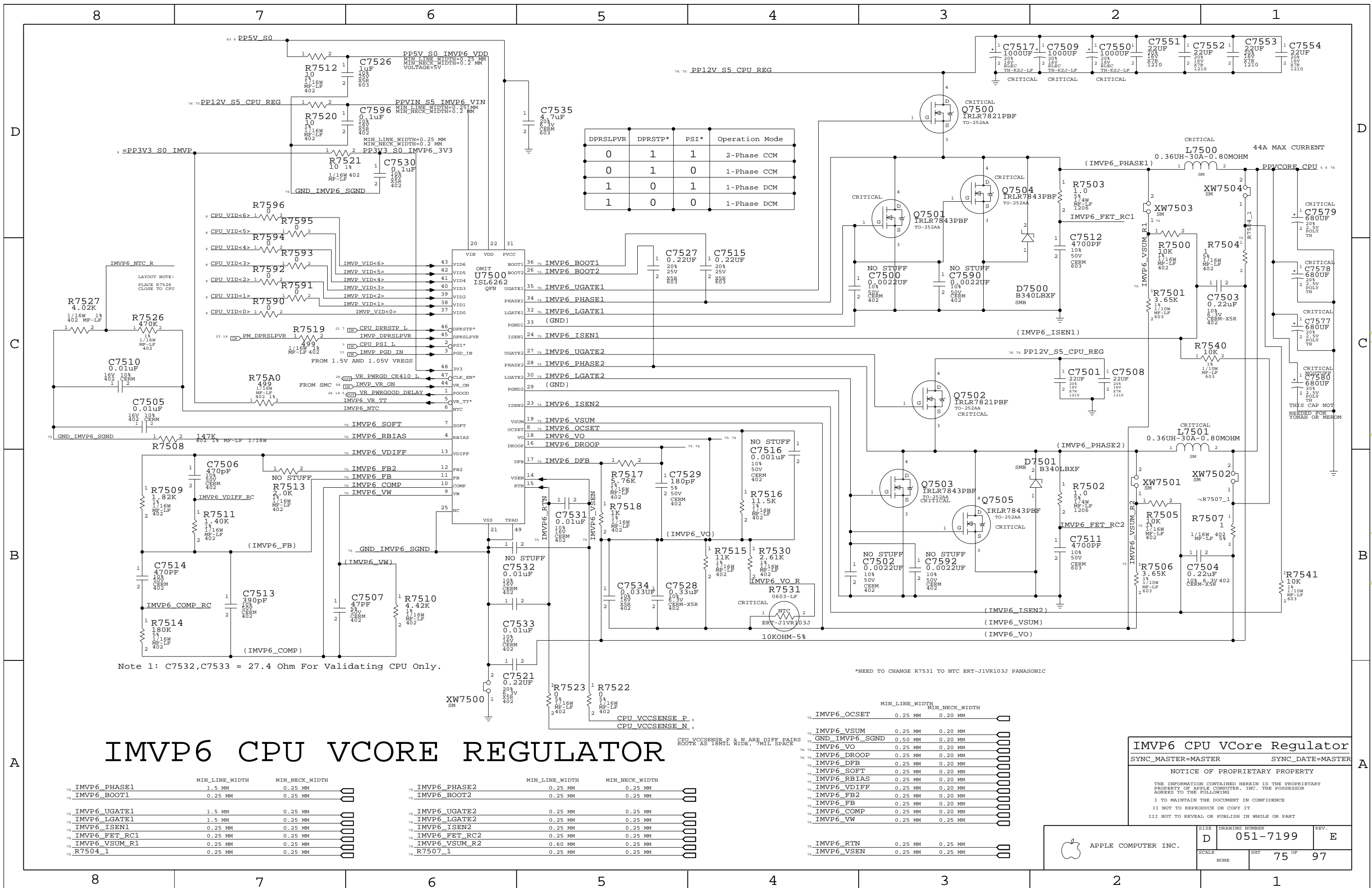
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
132S0099	1	CAPACITOR, .1UF, 0402	C7421	CRITICAL	CAMERA
11480315	1	RESISTOR, 10K OHM, 0402	C7421	CRITICAL	NOCAMERA

AUDIO: POWER SUPPLIES
 SYNC_MASTER=AUDIO SYNC_DATE=05/12/2006

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	D	051-7199	E
SCALE	SHT	74 OF	97
NONE			

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DPRSLPVR	DPRSTP*	PSI*	Operation Mode
0	1	1	2-Phase CCM
0	1	0	1-Phase CCM
1	0	1	1-Phase DCM
1	0	0	1-Phase DCM

Pin	Signal	Value
36	IMVP6_BOOT1	0.22uF
26	IMVP6_BOOT2	0.22uF
35	IMVP6_UGATE1	10% 25V
34	IMVP6_PHASE1	10% 25V
32	IMVP6_LGATE1	10% 25V
33	(GND)	
24	IMVP6_ISEN1	10% 25V
27	IMVP6_UGATE2	10% 25V
28	IMVP6_PHASE2	10% 25V
30	IMVP6_LGATE2	10% 25V
29	(GND)	
23	IMVP6_ISEN2	10% 25V
19	IMVP6_VSUM	10% 25V
8	IMVP6_OCSET	10% 25V
18	IMVP6_VO	10% 25V
16	IMVP6_DROOP	10% 25V
17	IMVP6_DFB	10% 25V
14	VSEN	10% 25V
15	RTN	10% 25V
21	IMVP6_VSEN	10% 25V
49	IMVP6_VSEN	10% 25V
75	IMVP6_VSEN	10% 25V
25	NC	
21	VSS	
49	TPAD	

IMVP6 CPU VCore Regulator

Pin	Signal	MIN_LINE_WIDTH	MIN_NECK_WIDTH
75	IMVP6_PHASE1	1.5 MM	0.25 MM
75	IMVP6_BOOT1	0.25 MM	0.25 MM
75	IMVP6_UGATE1	1.5 MM	0.25 MM
75	IMVP6_LGATE1	1.5 MM	0.25 MM
75	IMVP6_ISEN1	0.25 MM	0.25 MM
75	IMVP6_FET_RC1	0.25 MM	0.25 MM
75	IMVP6_VSUM_R1	0.25 MM	0.25 MM
75	R7504_1	0.25 MM	0.25 MM

Pin	Signal	MIN_LINE_WIDTH	MIN_NECK_WIDTH
75	IMVP6_PHASE2	0.25 MM	0.25 MM
75	IMVP6_BOOT2	0.25 MM	0.25 MM
75	IMVP6_UGATE2	0.25 MM	0.25 MM
75	IMVP6_LGATE2	0.25 MM	0.25 MM
75	IMVP6_ISEN2	0.25 MM	0.25 MM
75	IMVP6_FET_RC2	0.25 MM	0.25 MM
75	IMVP6_VSUM_R2	0.60 MM	0.25 MM
75	R7507_1	0.25 MM	0.25 MM

Pin	Signal	MIN_LINE_WIDTH	MIN_NECK_WIDTH
75	IMVP6_OCSET	0.25 MM	0.20 MM
75	IMVP6_VSUM	0.25 MM	0.20 MM
75	GND_IMVP6_SGND	0.50 MM	0.20 MM
75	IMVP6_VO	0.25 MM	0.20 MM
75	IMVP6_DROOP	0.25 MM	0.20 MM
75	IMVP6_DFB	0.25 MM	0.20 MM
75	IMVP6_SOFT	0.25 MM	0.20 MM
75	IMVP6_RBIAS	0.25 MM	0.20 MM
75	IMVP6_VDIFF	0.25 MM	0.20 MM
75	IMVP6_FB2	0.25 MM	0.20 MM
75	IMVP6_FB	0.25 MM	0.20 MM
75	IMVP6_COMP	0.25 MM	0.20 MM
75	IMVP6_VW	0.25 MM	0.25 MM
75	IMVP6_RTN	0.25 MM	0.25 MM
75	IMVP6_VSEN	0.25 MM	0.25 MM

IMVP6 CPU VCore Regulator
 SYNC_MASTER=MASTER SYNC_DATE=MASTER

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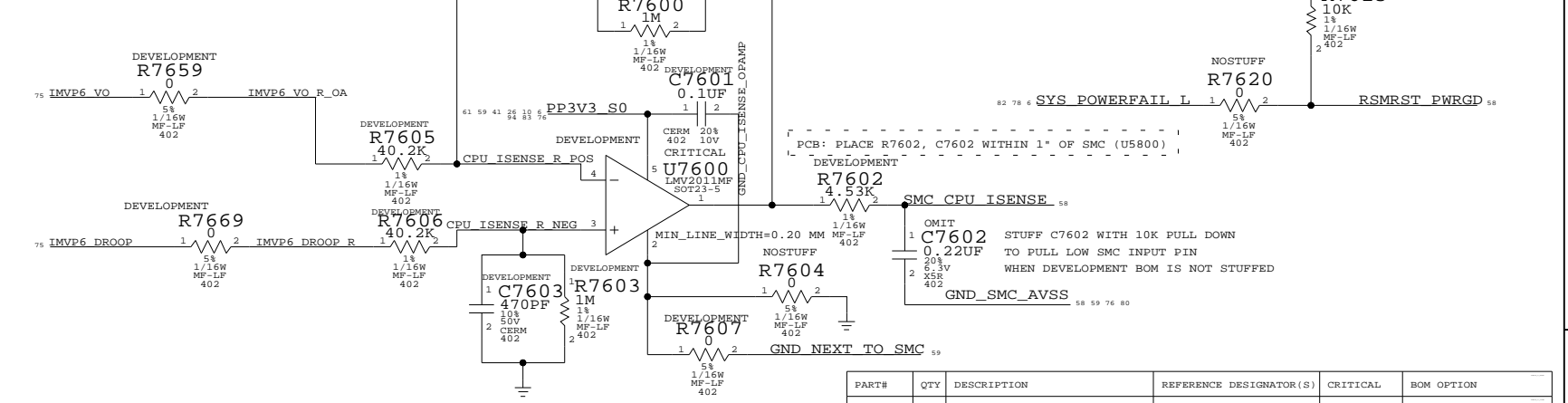
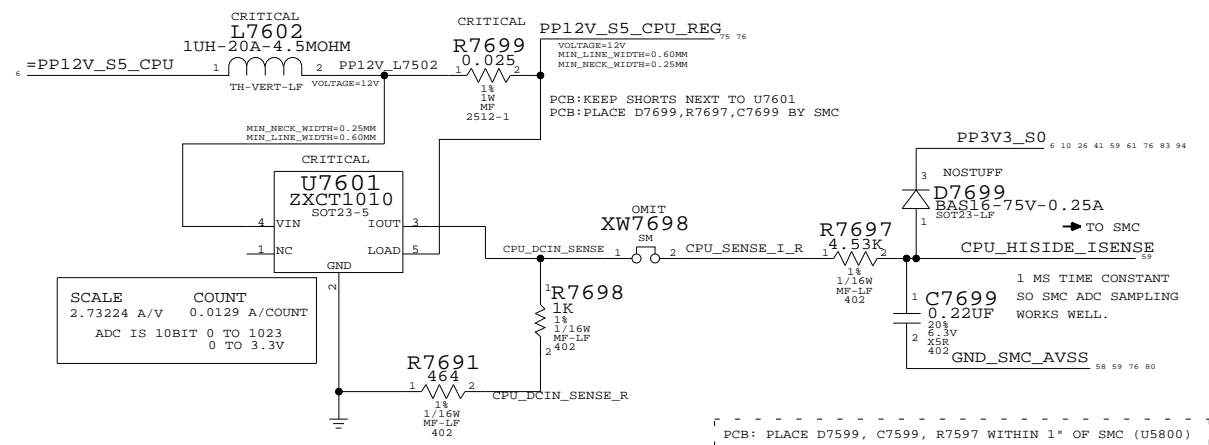
APPLE COMPUTER INC.	SIZE: D	DRAWING NUMBER: 051-7199	REV.: E
	SCALE: NONE	SHEET: 75 OF 97	

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PROCESSOR VCORE CURRENT SENSE
(USING 12V INPUT CURRENT TO DERIVE CPU CURRENT)

PROCESSOR VCORE CURRENT SENSE
(MEASURING DC/DC INDUCTOR DCR TO DERIVE CPU CURRENT)

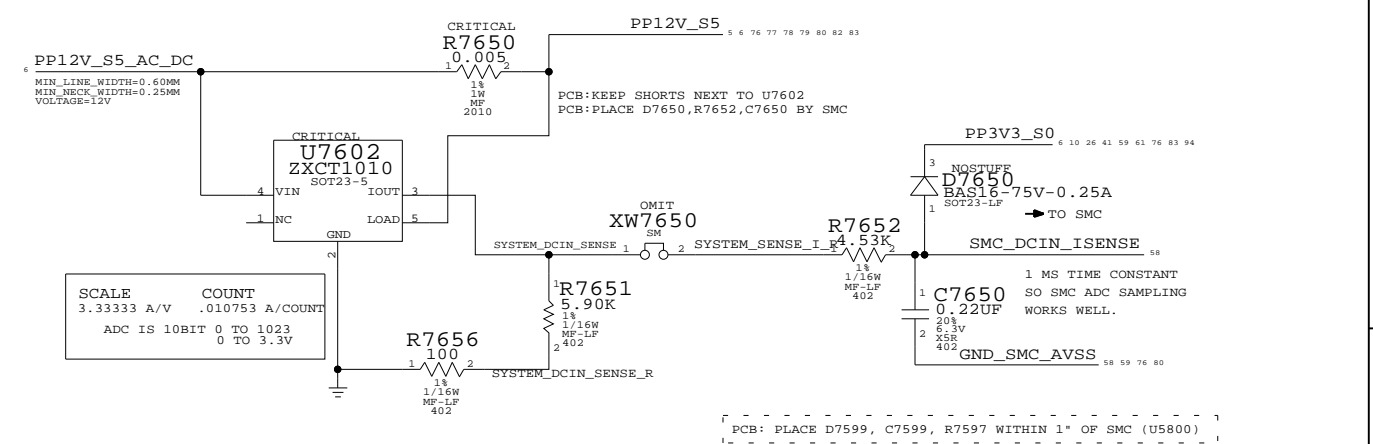
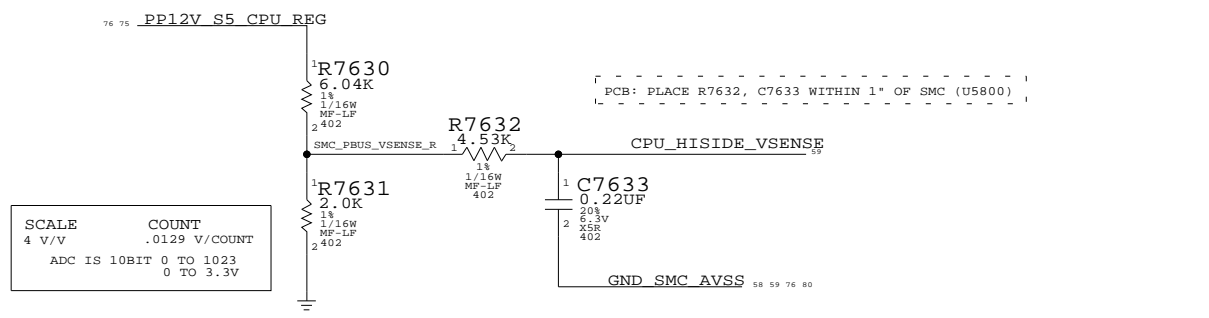
SMC PWRGD PULLUP



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
132S0080	1	CAP, 0.22UF, 6.3V, 20%, 0402	C7602		DEVELOPMENT
116S0090	1	RES, 10K, 5%, 0402	C7602		NOT_DEVELOPMENT

PROCESSOR DCIN VOLTAGE SENSE
(SCALING 12V INPUT VOLTAGE TO SMC)

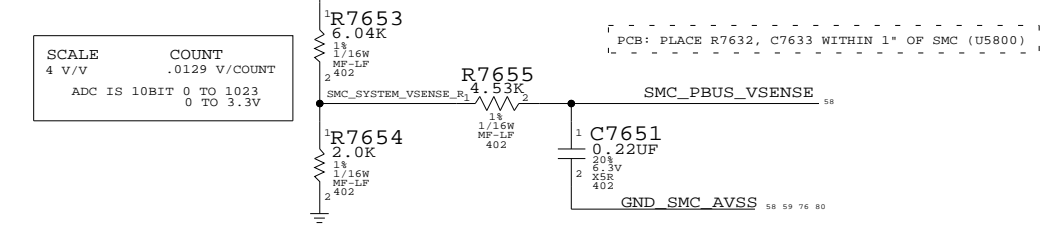
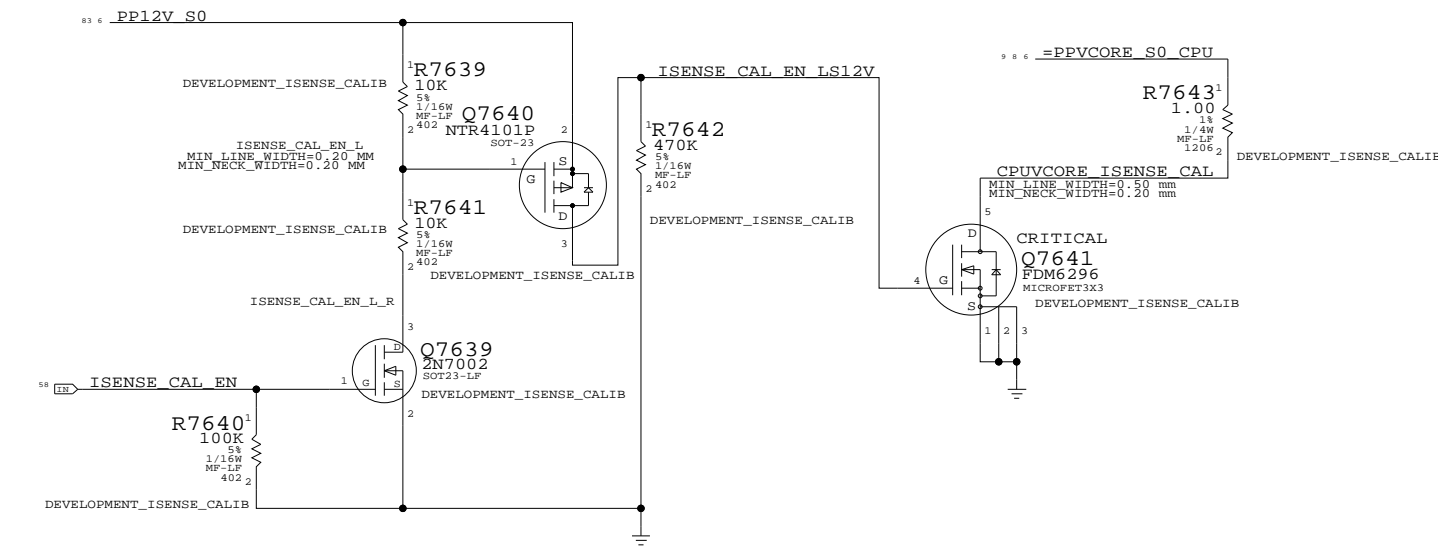
SYSTEM CURRENT SENSE



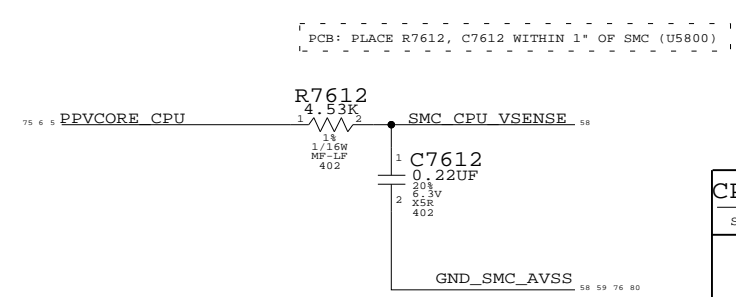
SYSTEM VOLTAGE SENSE
(SCALING 12V INPUT VOLTAGE TO SMC)

Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits



PROCESSOR VCORE SENSE



CPU & SYSTEM SENSE CIRCUITRIES

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

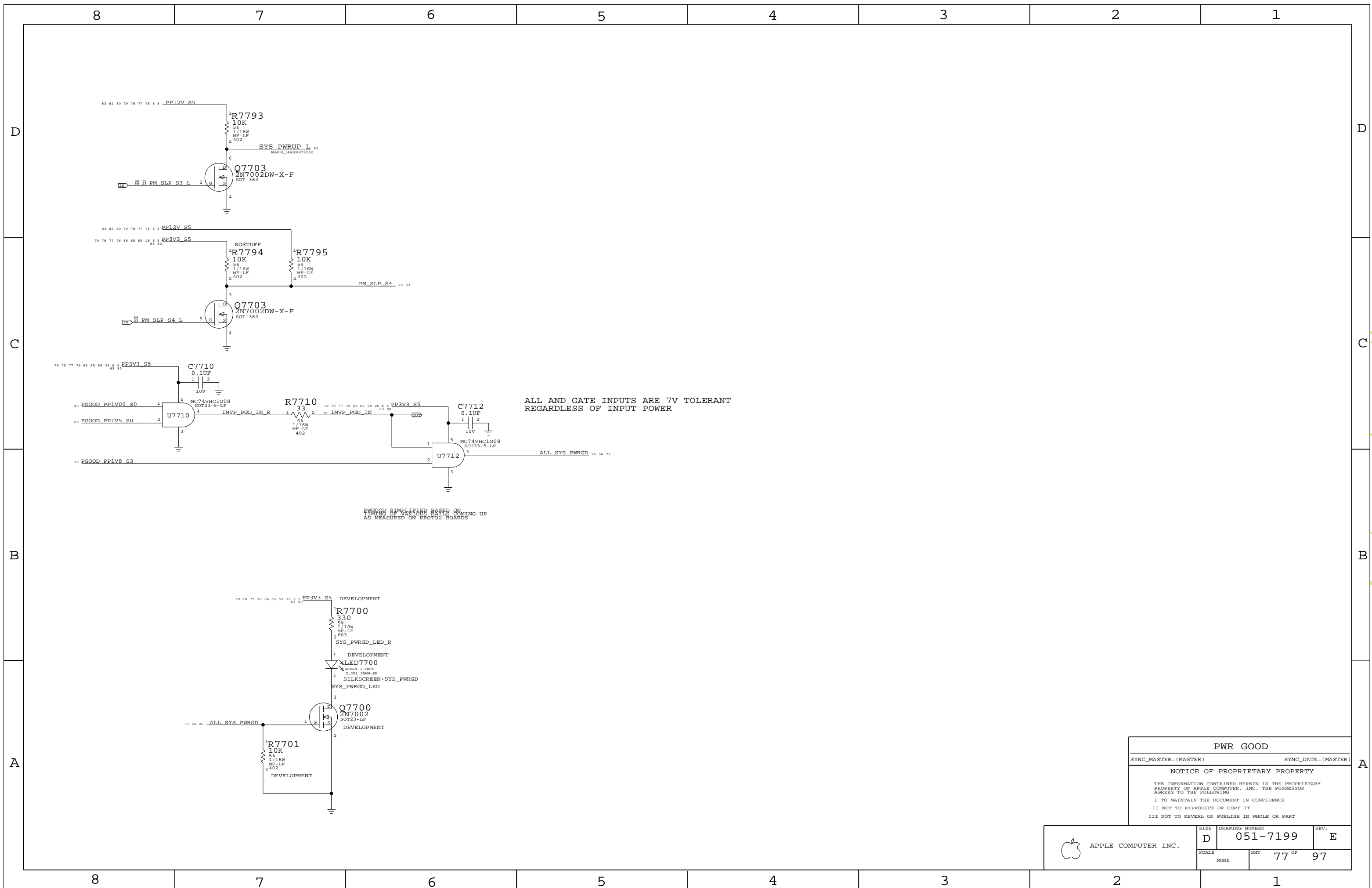
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	D	051-7199	E
SCALE	SHT	76 OF	97
NONE			



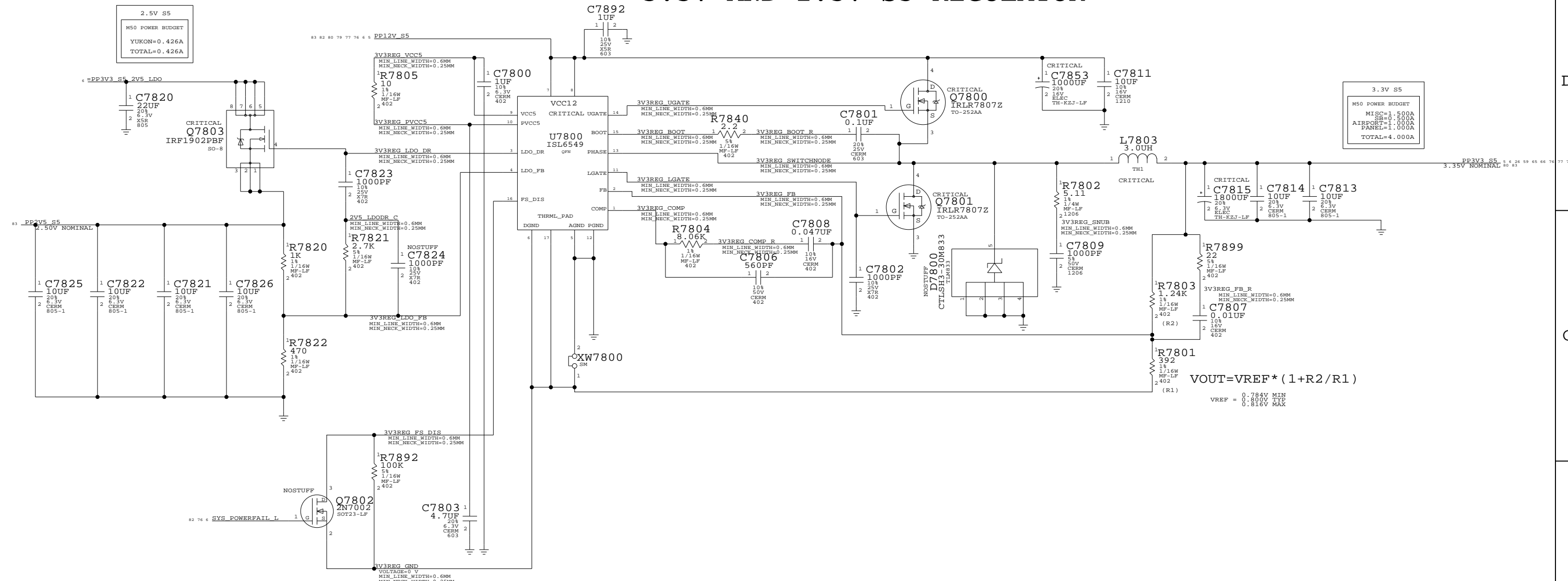
ALL AND GATE INPUTS ARE 7V TOLERANT
REGARDLESS OF INPUT POWER

PWGOOD SIMPLIFIED BASED ON
TIMING OF VARIOUS RAILS COMING UP
AS MEASURED ON PROTO2 BOARDS

PWR GOOD
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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	SCALE NONE	SHEET 77 OF 97	

3.3V AND 2.5V S5 REGULATOR



$V_{OUT} = V_{REF} * (1 + R2/R1)$
 $V_{REF} = 0.784V \text{ MIN}$
 $0.800V \text{ TYP}$
 $0.816V \text{ MAX}$

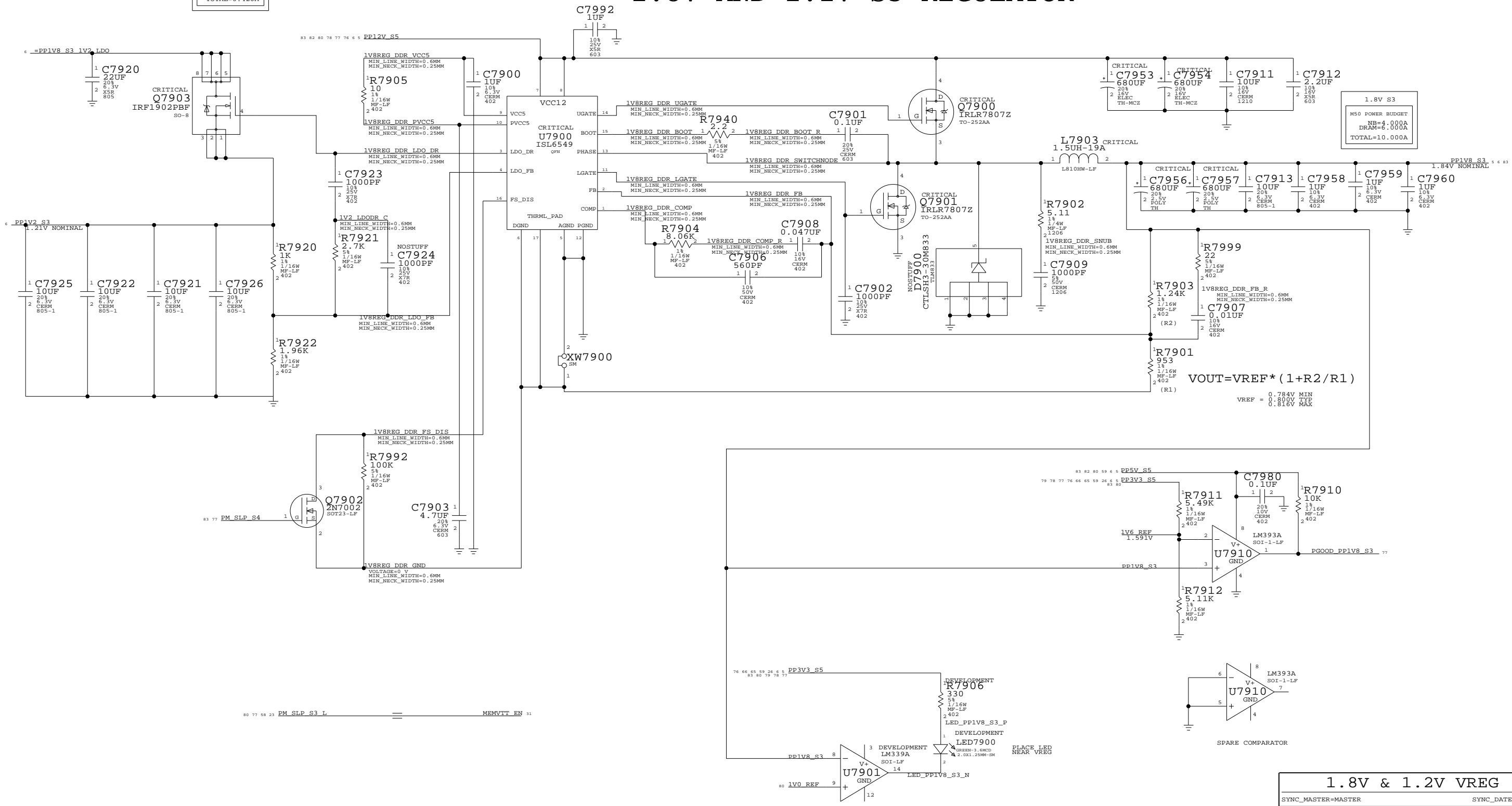
3V DC/DC 2.5V
 SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)
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	D	051-7199	E
SCALE	SHT	78 OF 97	
NONE		TRUE	

1.8V AND 1.2V S3 REGULATOR

1.2V S3
MS0 POWER BUDGET
YUKON=0.426A
TOTAL=0.426A

1.8V S3
MS0 POWER BUDGET
NB=4.000A
DRAM=6.000A
TOTAL=10.000A



1.8V & 1.2V VREG

SYNC_MASTER=MASTER SYNC_DATE=MASTER

NOTICE OF PROPRIETARY PROPERTY

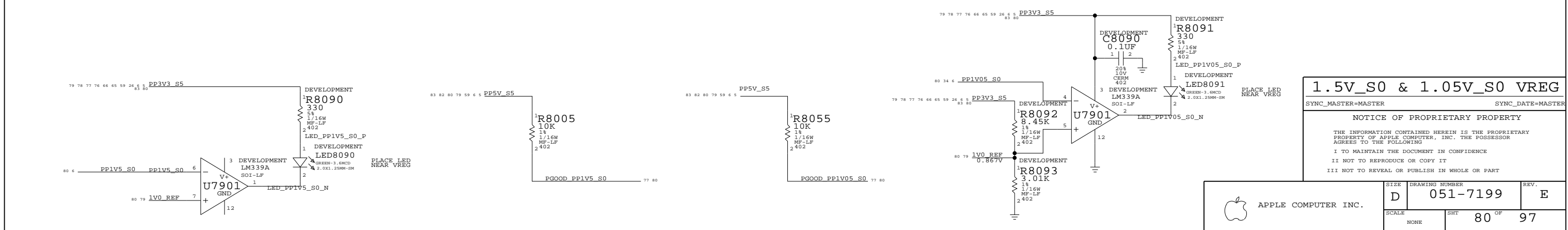
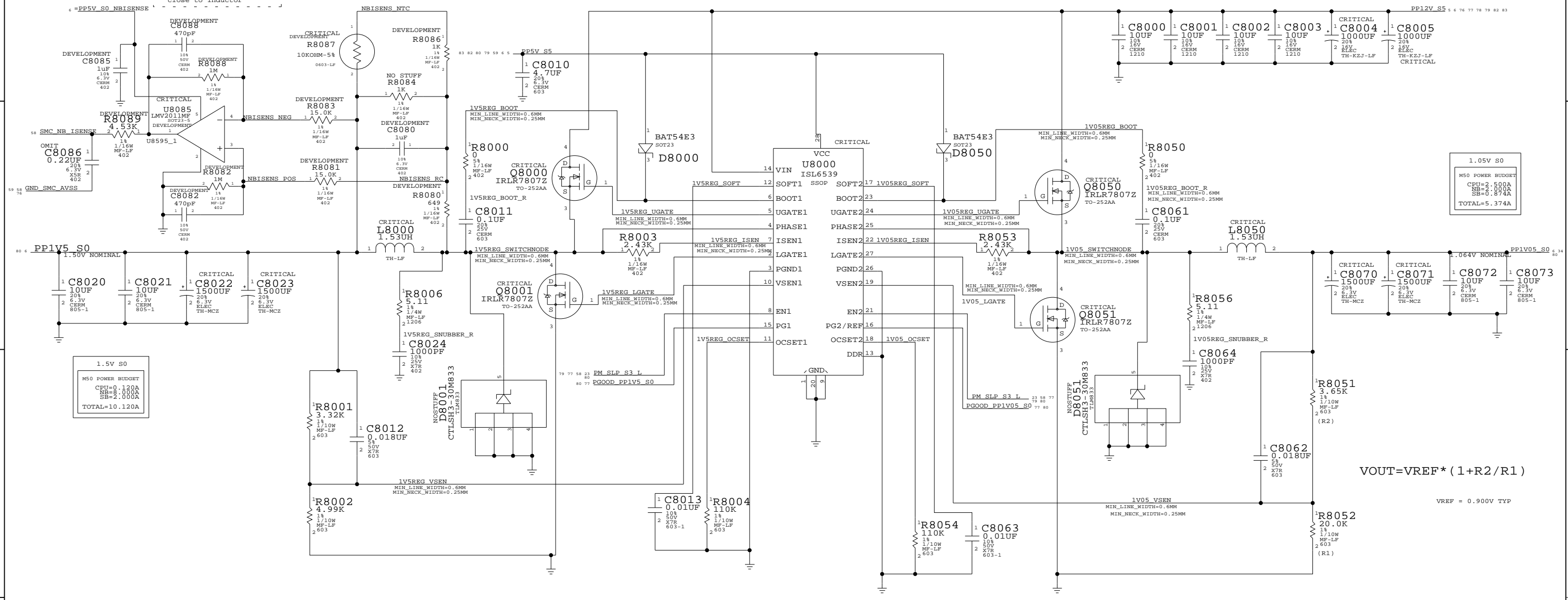
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	D	051-7199	E
SCALE	SHT	79 OF	97
NONE			

1.5V S0 AND 1.05V S0 RAILS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
13280080	1	CAP,0.22UF,6.3V,20%,0402	C8086		DEVELOPMENT
11650090	1	RES,10K,5%,0402	C8086		NOT_DEVELOPMENT

Placement Note:
KEEP C8080, R8080,
R8084 AND R8087
close to inductor



1.5V_S0 & 1.05V_S0 VREG

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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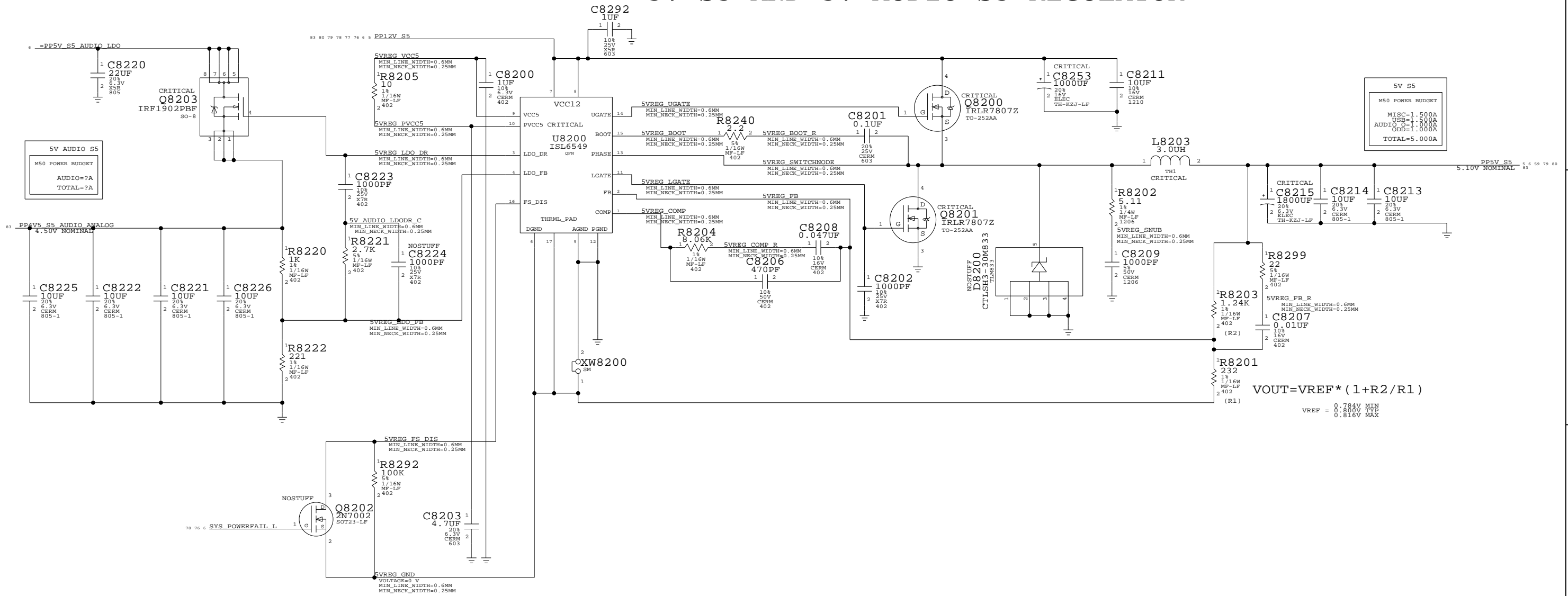
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	D	051-7199	E
SCALE	SHT	80 OF	97
NONE			

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5V S5 AND 5V AUDIO S5 REGULATOR



POWER SUPPLY 3.3V/5V MAIN SWITCH

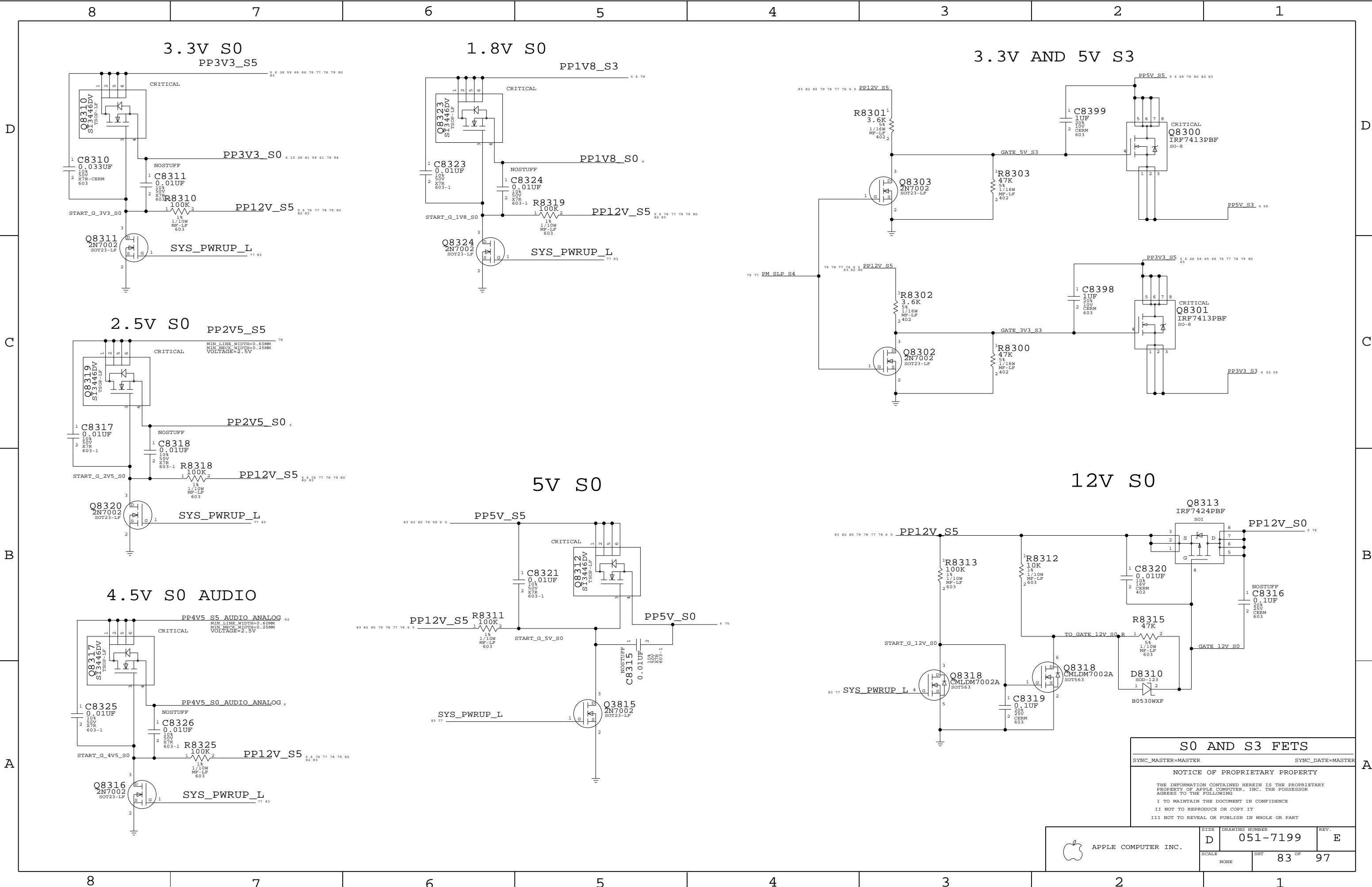
5V DC/DC

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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	D	051-7199	E
SCALE	SHT	82 OF	97
NONE			



S0 AND S3 FETS

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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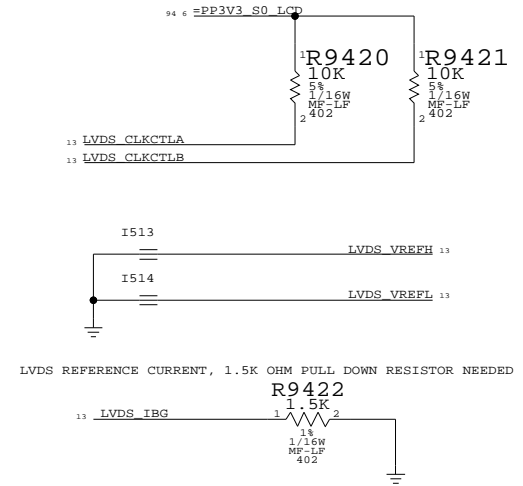
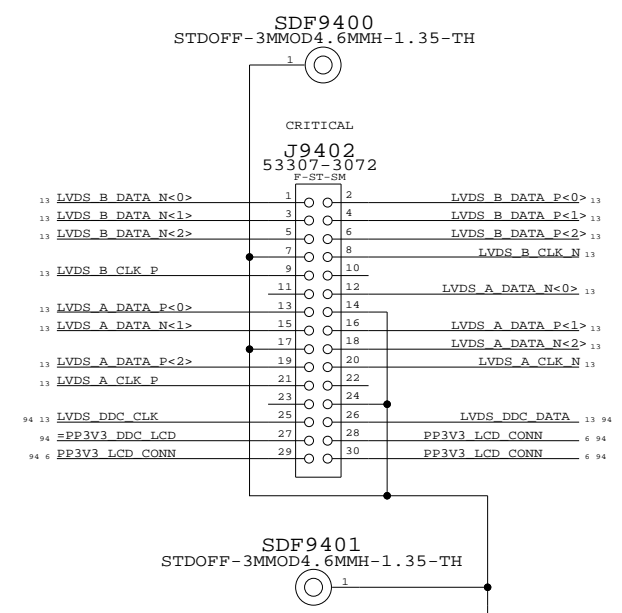
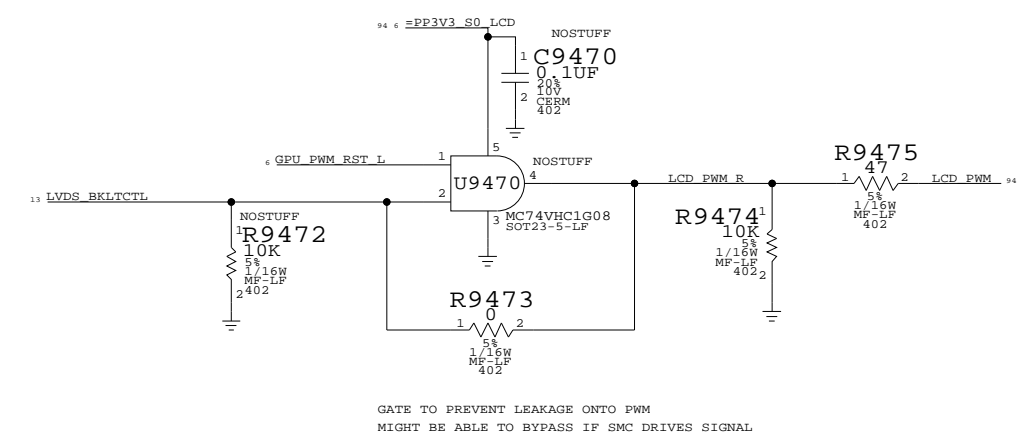
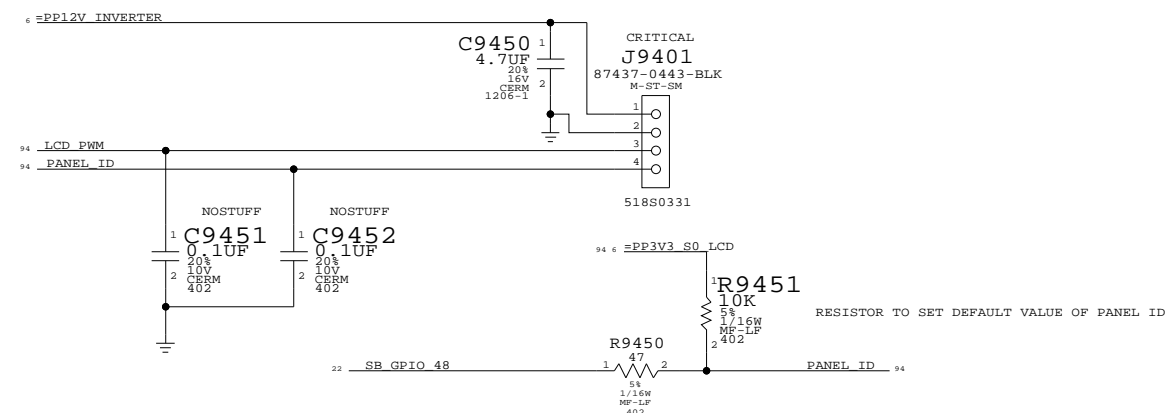
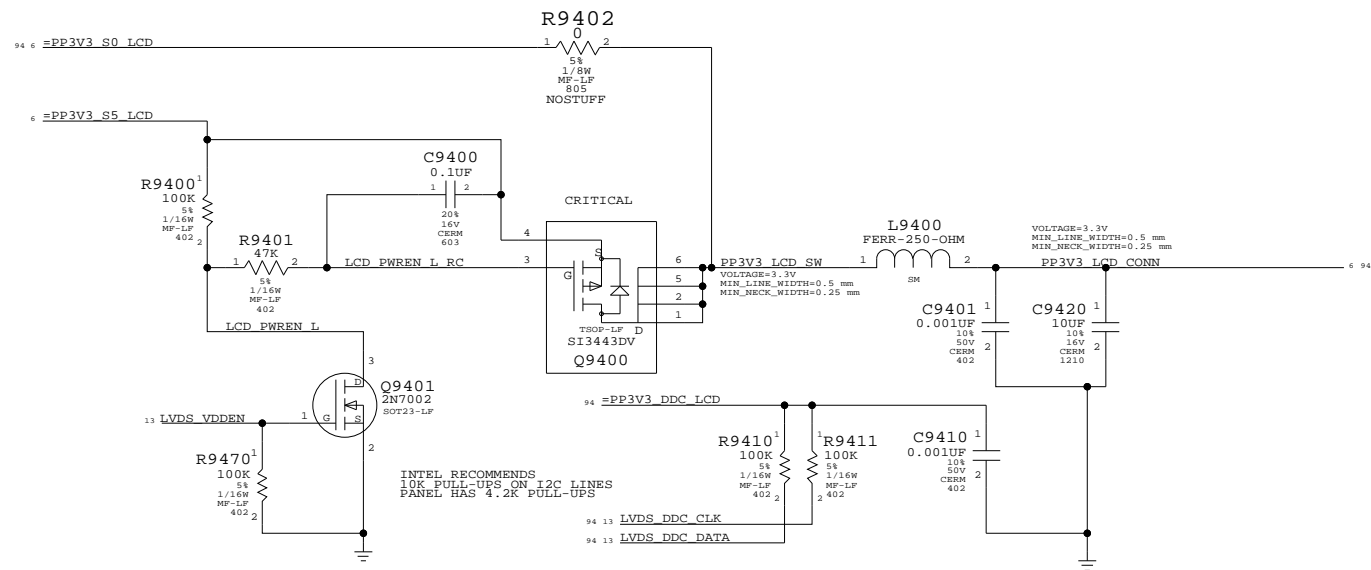
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7199	REV. E
	SCALE NONE	SHEET 83 OF 97	

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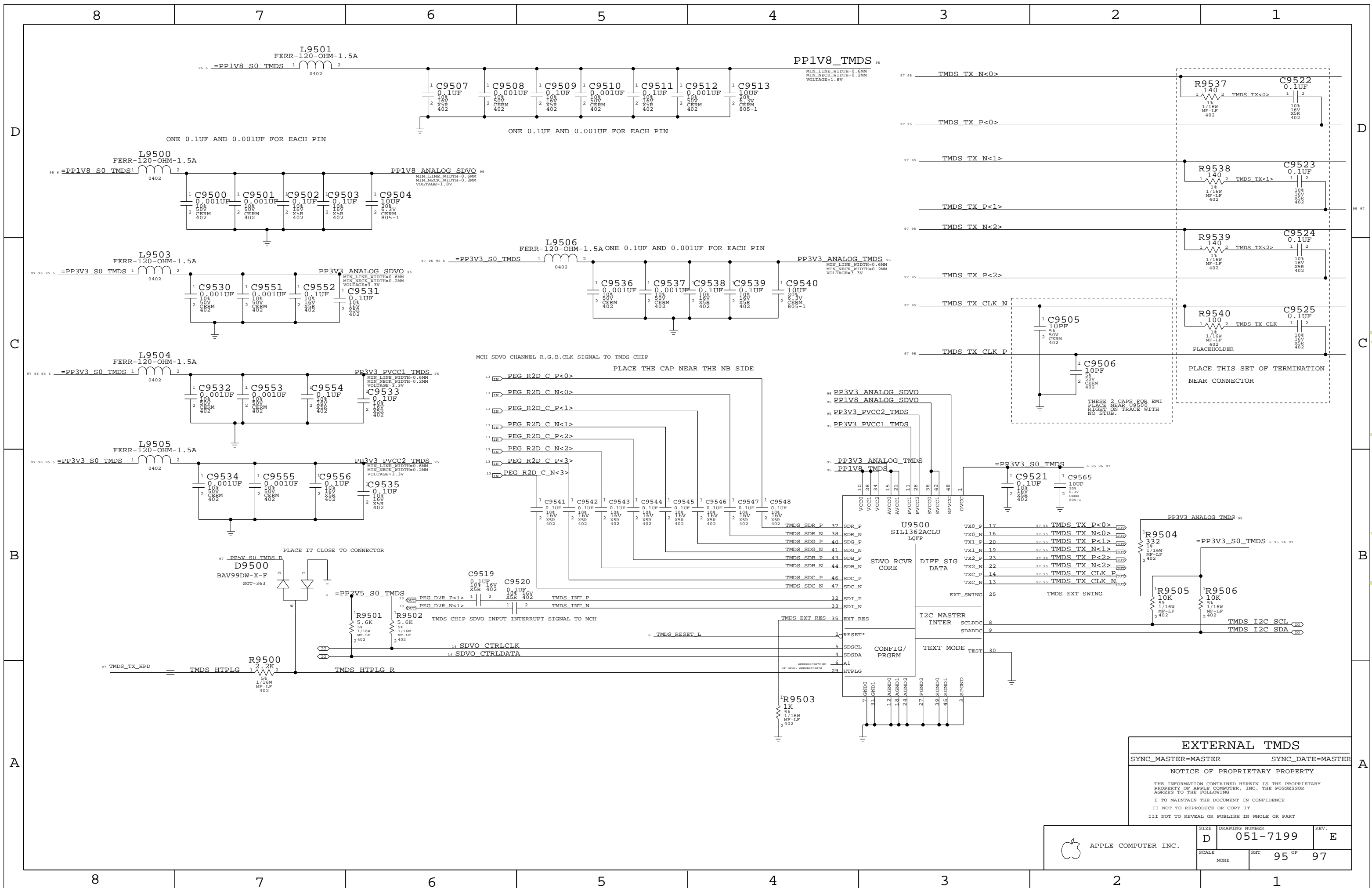
LCD (LVDS) INTERFACE

INVERTER INTERFACE



Internal Display Conns	
SYNC_MASTER=MASTER	SYNC_DATE=MASTER
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7199	E
SCALE	SHT	94 OF	97
NONE			



EXTERNAL TMD5

SYNC_MASTER=MASTER SYNC_DATE=MASTER

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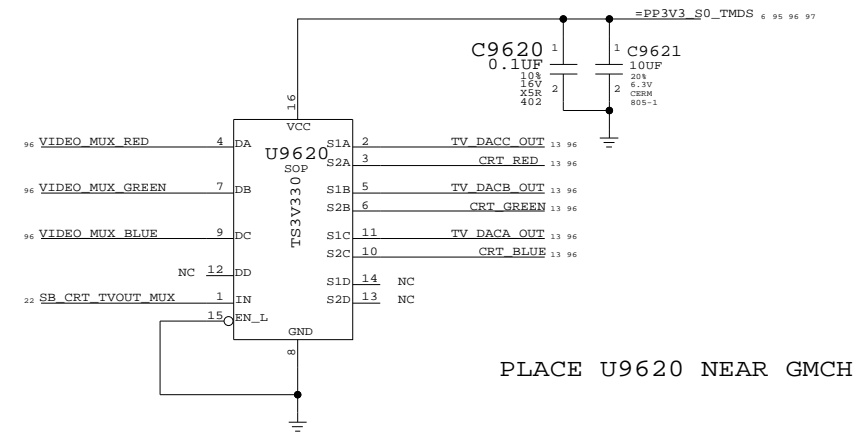
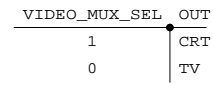
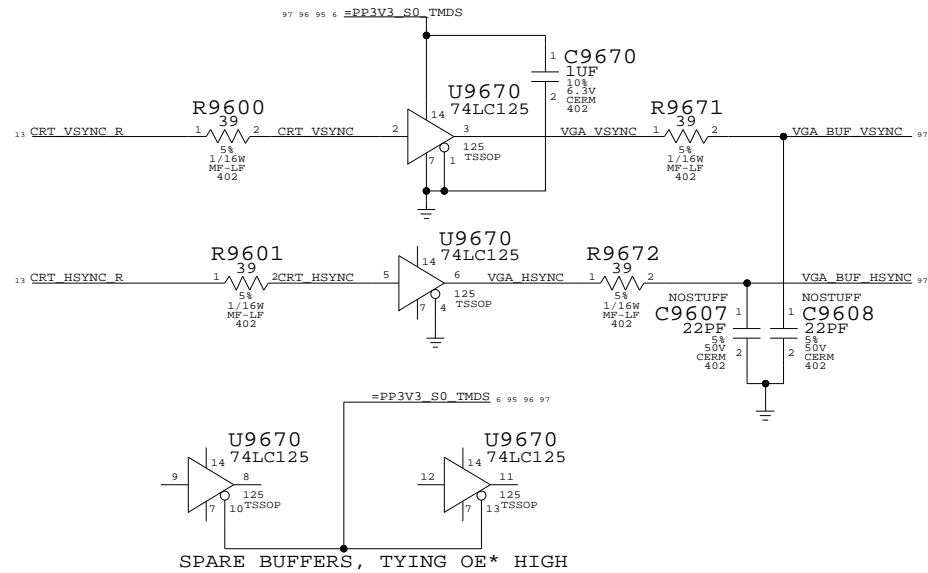
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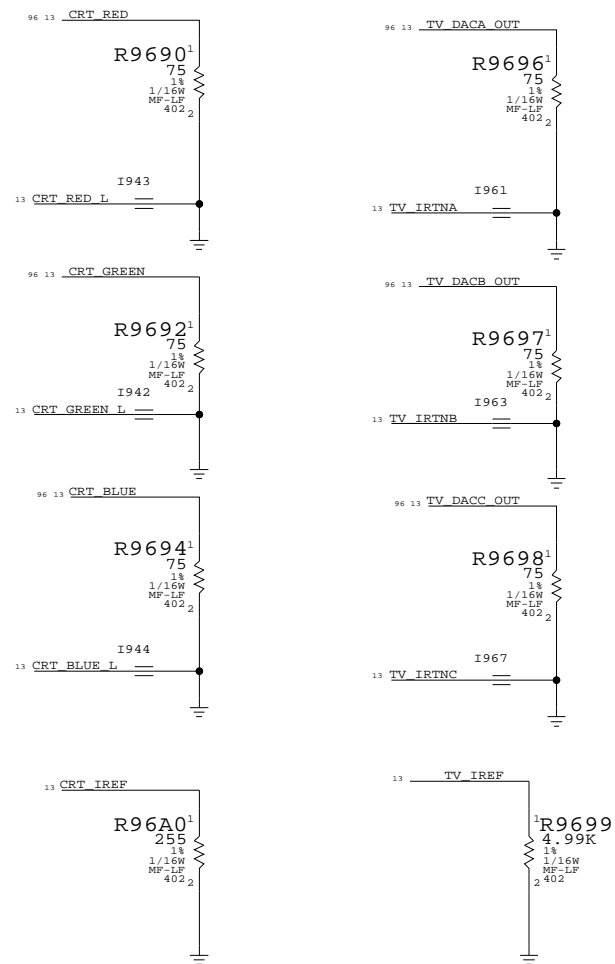
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7199	REV. E
	SCALE NONE	SHEET 95 OF 97	

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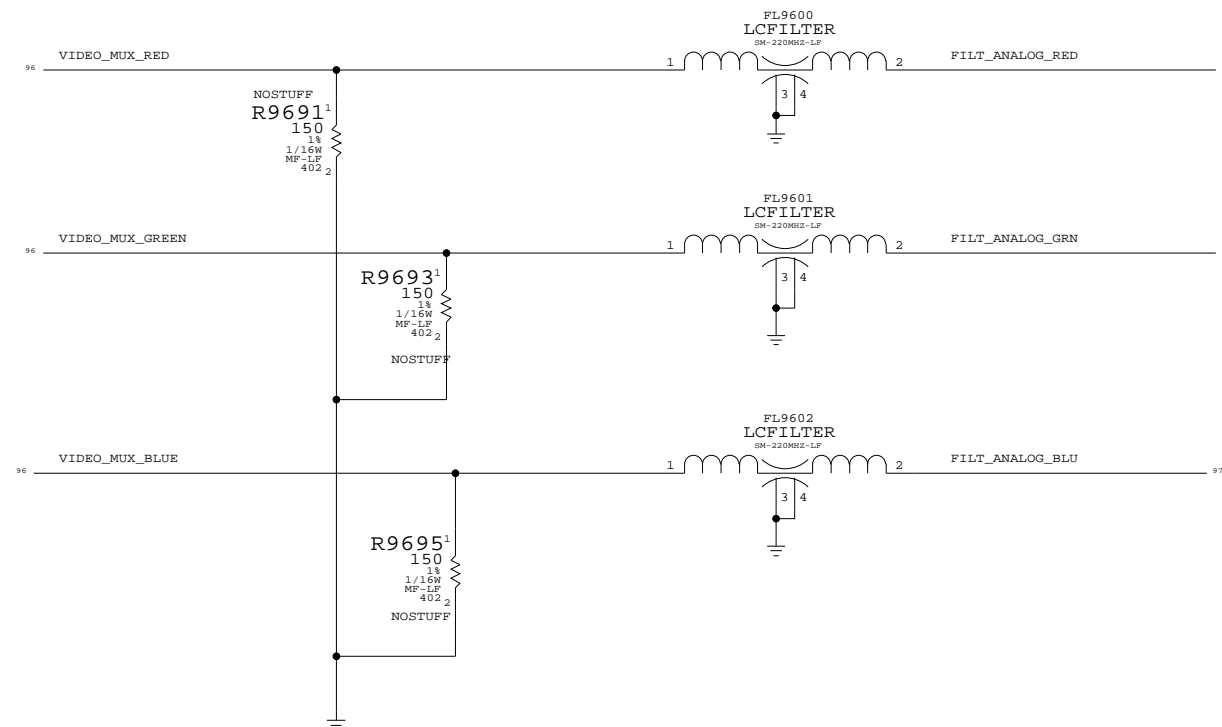
VGA SYNC BUFFERS



PLACE RESISTORS AT NORTHBRIDGE



ANALOG FILTERING PLACE BY CONNECTOR



TMDS/Inverter/ExtVGA
 SYNC_MASTER=MASTER SYNC_DATE=MASTER

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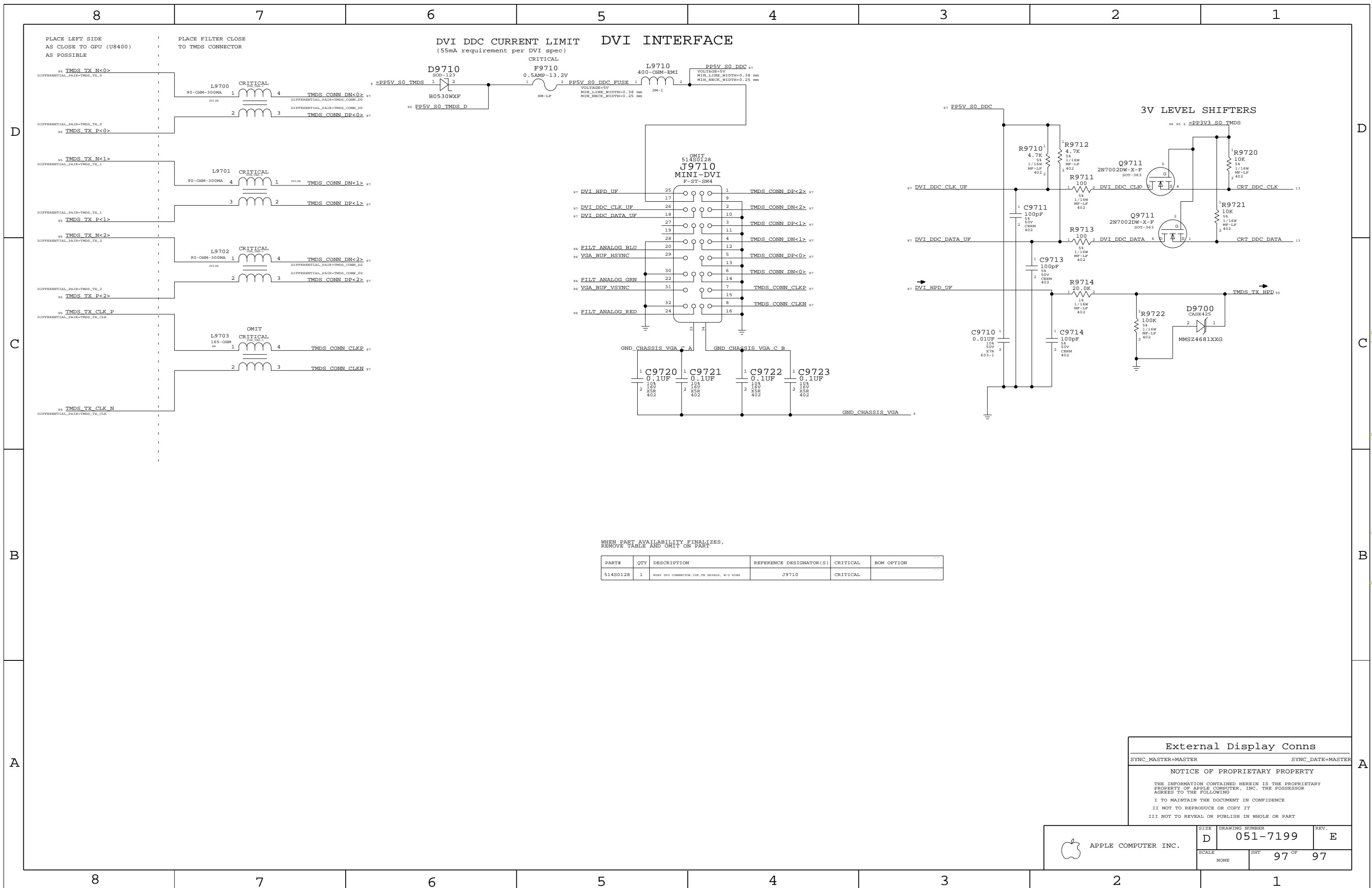
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SCALE	SHT	96 OF	97
NONE			



WHEN PART AVAILABILITY FINALIZES,
REMOVE TABLE AND OMIT ON PART

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514S0128	1	MINI DVI CONNECTOR, 16P, TR SHIELD, W/O BIAS	J9710	CRITICAL	

External Display Conns
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