1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
C	0001188998	PRODUCTION RELEASED	2011-07-22

J59
(7/22/2011)

DRAWING TITLE: SCH,J59,MLB

Apple Inc.

DRAWING NUMBER: 051-8774 | SIZE: D

REVISION: C.0.0

BRANCH:

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SYNC_MASTER=MASTER SYNC_DATE=N/A

PAGE TITLE

J59 BLOCK DIAGRAM

Apple Inc.

DRAWING NUMBER 051-8774 SIZE D

REVISION C.0.0

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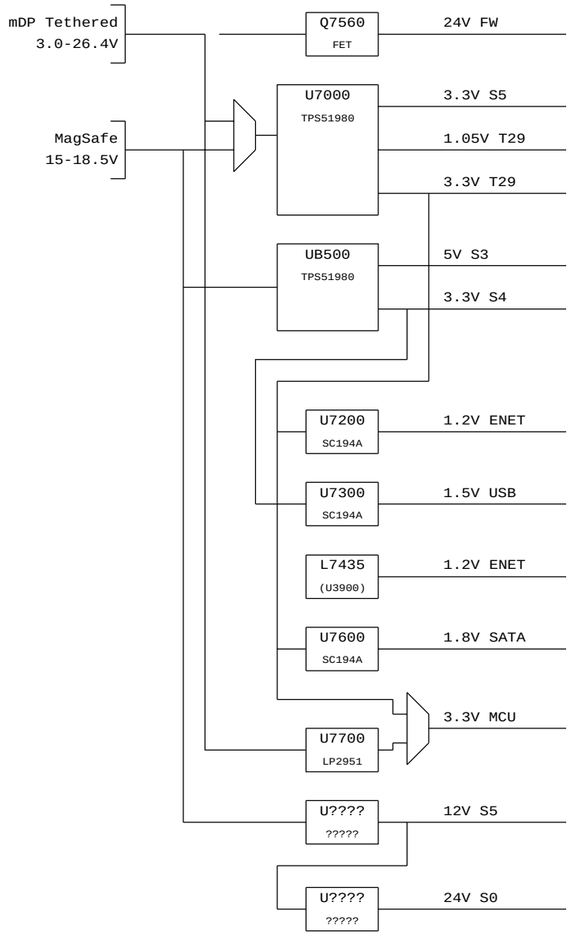

Device Function:	Dr.B	Mr.Dev	Mr.Dev	Mr.Dev	Display	ENET	FW	SATA	DPIn
Power Source:	Self	Self	Bus	Bus	Self	Bus	Bus	Bus	Bus
Wake Support:	Yes	Yes	Yes	No	Yes	Yes	No	No	No
24V FW	FW (420mA / 10W)	FW (420mA)	FW (420mA)	FW (420mA)	FW (420mA)	N/A	FW (420mA)	N/A	N/A
3.3V S5	MCU (10mA)	MCU (10mA)	N/A	N/A	MCU (10mA)	N/A	N/A	N/A	N/A
1.05V T29	RTRx2,FW,SATA	RTR,FW,SATA	RTR,FW,SATA	RTR,FW,SATA	RTRx2,FW	RTR	RTR,FW	RTR,SATA	RTR
3.3V T29	RTRx2,FW,SATA	RTR,FW,SATA	RTR,FW,SATA	RTR,FW,SATA	RTRx2,FW	RTR	RTR,FW	RTR,SATA	RTR,mDP
5V S3	USB (2.1A)	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
3.3V S4	mDPx2 (1A)	mDPx2 (1A)	N/A	N/A	mDP (1A)	N/A	N/A	N/A	N/A
1.2V ENET	DP++ (440mA)	DP++ (440mA)	N/A	N/A	DP++ (440mA)	N/A	N/A	N/A	N/A
1.5V USB	PLX (USB) (210mA)	PLX (USB) (210mA)	N/A	N/A	PLX (USB) (210mA)	N/A	N/A	N/A	N/A
1.2V ENET	N/A	N/A	ENET (400mA?)	N/A	N/A	ENET (400mA?)	N/A	N/A	N/A
1.8V SATA	SATA (250mA)	SATA (250mA)	SATA (250mA)	SATA (250mA)	N/A	N/A	N/A	SATA (250mA)	N/A
3.3V MCU	N/A	N/A	MCU (10mA)	MCU (10mA)	N/A	MCU (10mA)	MCU (10mA)	MCU (10mA)	MCU (10mA)

T29 Bus-Powered Device Power States:

S4: Device negotiation, SRC_PWR = 3.0-3.6V (MCU function only)
S3: Device sleep, SRC_PWR = 5.0-26.4V (optional wake functions supported)
S0: Device running, SRC_PWR = 21.6-26.4V (run functions supported)

NOTE: Devices not supporting wake function would not implement S3 state.

T29 Self-Powered Device Power States:

S5: Device standby, no cable attached (MCU function & DP port power only)
S3: Device sleep, cable attached (optional wake functions supported)
S0: Device running, cable attached (run functions supported)

DP/T29 Display-Specific Power States:

(In addition to S5-S0 states for T29 Self-Powered Device)
D5: Display standby, no cables attached
D3: Display sleep, DP cable detached or no source power, USB VBus present (USB wake supported)
D2: Display low-power, DP cable attached and source powered, source asleep per AUX command to TCON (USB wake supported)
D0: Display ready, DP cable attached and source powered

NOTEs:
- D5 implies S5, S0 implies D0.
- If only native DP source is attached, any Dx state can be supported while T29 is in S5.

NOTE: D2 not supported on Dr.B as there is no direct connection from panel TCON

SYNC_MASTER=MASTER SYNC_DATE=N/A
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Apple Inc.
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BOM NUMBER	BOM NAME	BOM OPTIONS
639-1575	PCBA,MLB,J59	BASIC
085-2422	PCBA,MLB,DEV,J59	DEVELOPMENT

BOM GROUP	BOM OPTIONS
BASIC	COMMON,ALTERNATE,T29HV:P12V,BIT_BANG_I2C,ENET_WAKE:PCIE,PIUSB_REV:B,PRODUCTION

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S0945	1	IC,T29-PRQ,220 FCBGA,15X15MM	U3600	CRITICAL	
338S0753	1	IC,FW643-E,1394B PHY/OHCI LINK/PCI-E,12	U4100	CRITICAL	
343S0549	1	IC,ASIC,GBIT ENET,QFN-48,6X6,BCM57761 B0	U3900	CRITICAL	
338S0977	1	PCI EXPRESS TO USB 2.0 HOST CONTROLLER(REV B)	U4600	CRITICAL	

FLASH	PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
RAW: 335S0550	341T0376	1	IC,EEPROM,J59 PRIMARY,SPI,32KBIT,MLP8	U3690	CRITICAL	
RAW: 335S0800	341T0331	1	ENET FLASH,C-IV,NO SD,J59	U3990	CRITICAL	
RAW: 335S0559	341T0375	1	IC,EEPROM,FW643-E2 GUID,I2C,2KBIT,MLP8	U4290	CRITICAL	
RAW: 337S4115	341T0385	1	IC,MCU,32B,LPC1114,32KB/8KB,HVQFN33,J59	U5000	CRITICAL	
RAW: 337S4115	341T0385	1	IC,PRGRMD,LPC1114,T29 SUPER MCU,HVQFN33	U9330	CRITICAL	
RAW: 337S3558	341T0378	1	IC,PRGRMD,LPC2144,J59 SYSTEM MCU	U2617	CRITICAL	
RAW: 353S2320	341T0369	1	IC,PRGRMD,PNX0161,AUDIO/HID,TFBGA88	U1400	CRITICAL	

ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0977	376S0859		ALL	DIODESINC ALT FET
376S0972	376S0612		ALL	ROHM ALT FET
377S0107	377S0066		ALL	ON SEMI ALT RCLAMP
155S0431	155S0289		L1204	ALTERNATE CM CHOKE
376S1029	376S0953		ALL	ALTERNATE DC/DC FET
376S1030	376S0801		ALL	ALTERNATE DC/DC FET
376S1017	376S0612		ALL	ALTERNATE TOSH SS FET
377S0124	377S0057		ALL	ALTERNATE VARISTOR
152S1483	152S1376		ALL	ALTERNATE INDUCTOR
155S0691	155S0183		ALL	ALT BEAD FOR BL FILT
128S0262	128S0220		ALL	ADDS KEMET TO SANYO
138S0684	138S0660		ALL	ADDS MURATA TO TAIYO
155S0571	155S0309		ALL	ALTERNATE FERRITE
353S3477	353S3207		ALL	ALTERNATE FAB U9410

Schematic / PCB / EEEE #’s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
820-2997	1	PCBF,MLB,J59	PCB1	CRITICAL	
051-8774	1	SCH,MLB,J59	SCH1	CRITICAL	
825-7122	1	MLB LABEL, 48.0MM X 4.8MM	[EEEE_DHMY]	CRITICAL	

SYNC_MASTER=MASTER SYNC_DATE=N/A

PAGE TITLE

BOM Configuration & Misc

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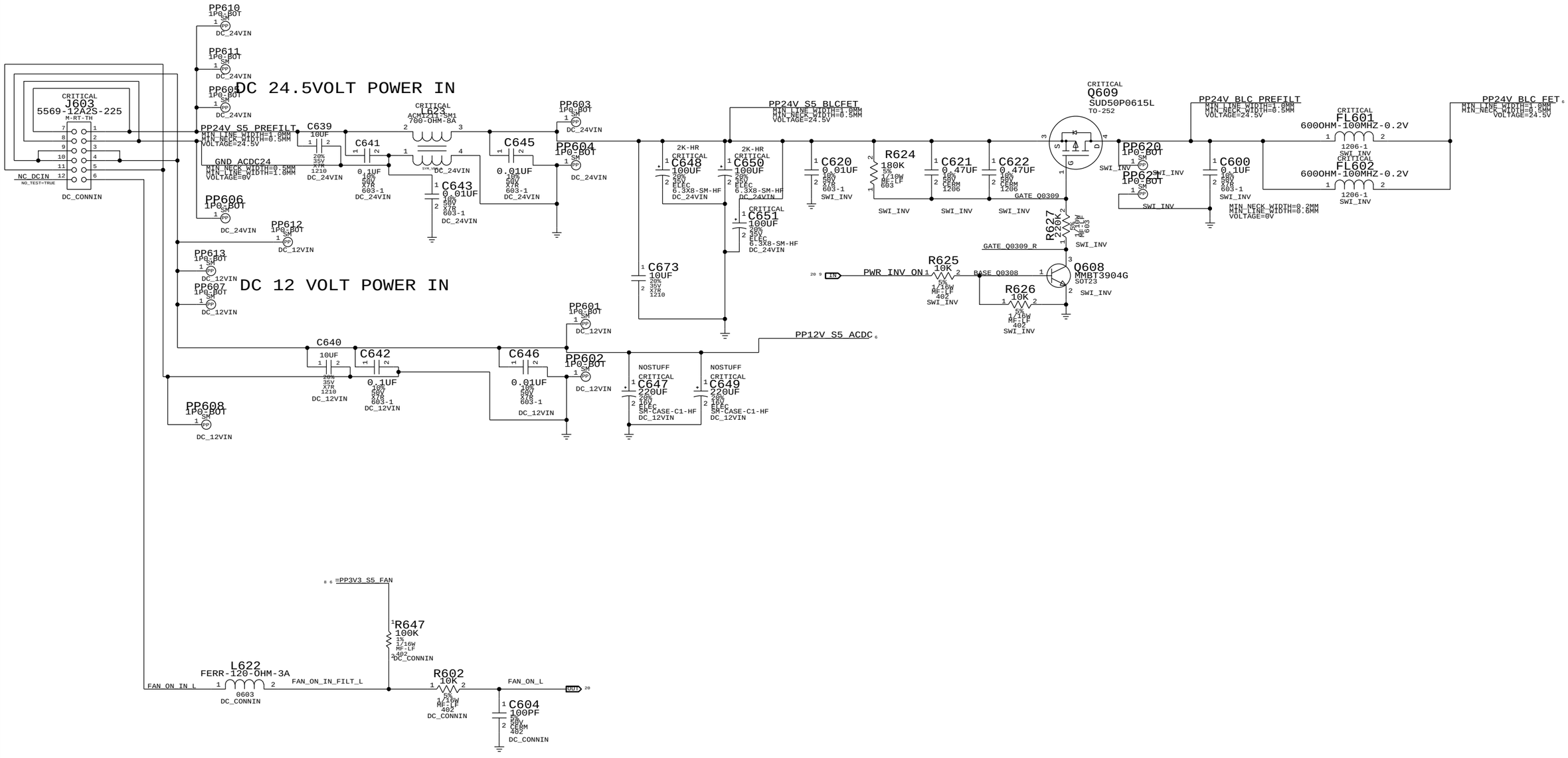
DC 24.5VOLT POWER IN

DC 12 VOLT POWER IN



SYNC_MASTER=MASTER	SYNC_DATE=N/A
PAGE TITLE	DC POWER IN
Apple Inc.	DRAWING NUMBER 051-8774 SIZE D
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S5 Rails

PP12V_S5
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=12V
MAKE_BASE=TRUE

PPVIN_SW_T29BST 37
VOLTAGE=12V

- PP12V_S5_ACDC 5
- =PP12V_S5_FANFET 19
- =PP12V_S5_5V3V_VREG 39
- =PP12V_S5_AUDIOFET 19
- =PP12V_S5_LCDFET 19
- =PP12V_S5_P12VS0FET 40
- =PPVIN_SW_T29BST 6 37

PP5V_S5
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=5V
MAKE_BASE=TRUE

- PP5V_S5_REG 39
- =PP5V_S5_USB 33
- =PP5V_S5_AUDIOFET 19
- =PP5V_S5_CAMFET 10
- =PP5V_S5_P1V05S0_VREG 36

PP3V3_S5
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE

- PP3V3_S5_REG 39
- =PP3V3_S4_DEVRESET 7
- =PP3V3_S5_FANBUF 19
- =PP3V3_S5_FAN 5 8
- =PP3V3_S5_USB 31 32 33
- =PP3V3_S5_LPC 20 35
- =PP3V3_S5_AUDIOFET 19
- =PP3V3_S5_TCON 21
- =PP3V3_S5_JTAG 11
- =PP3V3_S5_BLC 9
- =PP3V3_S5_ALS 35
- =PP3V3_S5_P3V3S3FET 40
- =PP3V3_S5_P3V3S0FET 40
- =PP3V3_S4_DPAPWRSW 7 43
- =PP3V3_S5_T29P

RT800
0
1 2
5%
1/10W
MF-LF
603
PP3V3_S4_MCU
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_S4_MCU 11 34

S3 RAILS

PP3V3_S3
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE

< 2100 mA

- =PP3V3_S3_FET 40
- =PP3V3_S3_ENET_PHY 20 25
- =PP3V3_S3_USB 7 32 35
- =PP3V3_S3_ENET_SYSCLK 22
- =PP3V3_S3_P1V0S3REG 38
- =P1V0S3_EN 38

PP1V0_S3
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1V
MAKE_BASE=TRUE

- PP1V0_S3_REG 38
- =PP1V0_S3_USB 32

S0 RAILS

PP24V_S0_BLC
MIN_LINE_WIDTH=1.0MM
MIN_NECK_WIDTH=0.5MM
VOLTAGE=24.5V
MAKE_BASE=TRUE

- PP24V_BLC_FET 5
- =PP24V_BLC_LEDS 9

PP12V_S0
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=12V
MAKE_BASE=TRUE

- =PP12V_S0_FET 40
- =PP12V_S0_FW 30
- =PP12V_S0_P1V05S0_VREG 36

PP3V3_S0
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE

- =PP3V3_S0_FET 40
- =PP3V3_S0_DEVRESET 7
- =PP3V3_S0_CK505 22
- =PP3V3_S0_T29P 7 11 23 24
- =PP3V3_S0_I2C_UC 35
- =PP3V3_S0_FWPHY 28 29 30
- =PPVDDIO_S0_T29P_CLK 22
- =PP3V3_S0_TCPWRSW 40 41
- =PP3V3_S0_ENET_PHY 20 26
- 400 mA? =PP3V3_S0_TCON 21 35
- =PP3V3_S0_I2C_T29 35

PP1V05_S0
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V
MAKE_BASE=TRUE

- PP1V05_S0_REG 36
- =PP1V05_S0_CK505 22
- =PP1V05_S0_T29P 24

Digital Ground

GND
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=0V

T29 PORT POWER VOLTAGE

1000 MA

PP15VR12V_S3
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=15V
MAKE_BASE=TRUE

- =PP15V_T29_REG 37
- =PPHV_SW_DPAPWRSW 43 500 MA

37 6 =PPVIN_SW_T29BST

CRITICAL
T29HV:P12V
R890
0.001
1 2
1%
1W
MF
0815-HF

T29HV:P12V
R895
0
5%
1/10W
MF-LF
402
2 1

T29BST_PWREN_DIV_L OUT 37

750 MA

PP3V3_SW_TCPWR
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V
MAKE_BASE=TRUE

- =PP3V3_S0_TCPWR_FET 41
- =PP3V3_S0_TCCONN 41 750 MA

SYNC_MASTER=MASTER SYNC_DATE=N/A

PAGE TITLE
Power Aliases

Apple Inc.

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PCIe Assignments

23 IN	PCIE_T29_R2D_C_P<0>	PCIE_USB_R2D_C_P (MAKE_BASE=TRUE)	OUT 32 46
23 IN	PCIE_T29_R2D_C_N<0>	PCIE_USB_R2D_C_N (MAKE_BASE=TRUE)	OUT 32 46
23 OUT	PCIE_T29_D2R_P<0>	PCIE_USB_D2R_P (MAKE_BASE=TRUE)	IN 32 46
23 OUT	PCIE_T29_D2R_N<0>	PCIE_USB_D2R_N (MAKE_BASE=TRUE)	IN 32 46
23 IN	T29_PCIE_RESET_L<0>	USB_RESET_L (MAKE_BASE=TRUE)	OUT 32
23 IN	PCIE_T29_R2D_C_P<1>	PCIE_ENET_R2D_C_P (MAKE_BASE=TRUE)	OUT 26 46
23 IN	PCIE_T29_R2D_C_N<1>	PCIE_ENET_R2D_C_N (MAKE_BASE=TRUE)	OUT 26 46
23 OUT	PCIE_T29_D2R_P<1>	PCIE_ENET_D2R_P (MAKE_BASE=TRUE)	IN 26 46
23 OUT	PCIE_T29_D2R_N<1>	PCIE_ENET_D2R_N (MAKE_BASE=TRUE)	IN 26 46
23 IN	T29_PCIE_RESET_L<1>	ENET_RESET_L (MAKE_BASE=TRUE)	OUT 26
23 IN	PCIE_T29_R2D_C_P<2>	PCIE_FW_R2D_C_P (MAKE_BASE=TRUE)	OUT 28 46
23 IN	PCIE_T29_R2D_C_N<2>	PCIE_FW_R2D_C_N (MAKE_BASE=TRUE)	OUT 28 46
23 OUT	PCIE_T29_D2R_P<2>	PCIE_FW_D2R_P (MAKE_BASE=TRUE)	IN 28 46
23 OUT	PCIE_T29_D2R_N<2>	PCIE_FW_D2R_N (MAKE_BASE=TRUE)	IN 28 46
23 IN	T29_PCIE_RESET_L<2>	FW_RESET_L (MAKE_BASE=TRUE)	OUT 28
23 IN	PCIE_T29_R2D_C_P<3>	NC_PCIE_T29_R2D_C_P3 (MAKE_BASE=TRUE NO_TEST=TRUE)	
23 IN	PCIE_T29_R2D_C_N<3>	NC_PCIE_T29_R2D_C_N3 (MAKE_BASE=TRUE NO_TEST=TRUE)	
23 OUT	PCIE_T29_D2R_P<3>	NC_PCIE_T29_D2R_P3 (MAKE_BASE=TRUE NO_TEST=TRUE)	
23 OUT	PCIE_T29_D2R_N<3>	NC_PCIE_T29_D2R_N3 (MAKE_BASE=TRUE NO_TEST=TRUE)	
23 IN	T29_PCIE_RESET_L<3>	NC_T29_PCIE_RESET_L3 (MAKE_BASE=TRUE NO_TEST=TRUE)	

INTERNAL DP PANEL AC COUPLING CAPS

44 7 IN	DP_INT_ML_C_P<0>	C900 0.1UF 10% 16V X5R 402	DP_INT_ML_P<0> OUT 21 44 48
44 7 IN	DP_INT_ML_C_N<0>	C901 0.1UF 10% 16V X5R 402	DP_INT_ML_N<0> OUT 21 44 48
44 7 IN	DP_INT_ML_C_P<1>	C902 0.1UF 10% 16V X5R 402	DP_INT_ML_P<1> OUT 21 44 48
44 7 IN	DP_INT_ML_C_N<1>	C903 0.1UF 10% 16V X5R 402	DP_INT_ML_N<1> OUT 21 44 48
44 7 IN	DP_INT_ML_C_P<2>	C904 0.1UF 10% 16V X5R 402	DP_INT_ML_P<2> OUT 21 44 48
44 7 IN	DP_INT_ML_C_N<2>	C905 0.1UF 10% 16V X5R 402	DP_INT_ML_N<2> OUT 21 44 48
44 7 IN	DP_INT_ML_C_P<3>	C906 0.1UF 10% 16V X5R 402	DP_INT_ML_P<3> OUT 21 44 48
44 7 IN	DP_INT_ML_C_N<3>	C907 0.1UF 10% 16V X5R 402	DP_INT_ML_N<3> OUT 21 44 48
44 7 IN	DP_INT_AUXCH_C_P	C908 0.1UF 10% 16V X5R 402	DP_INT_AUXCH_P OUT 21 44 48
44 7 IN	DP_INT_AUXCH_C_N	C909 0.1UF 10% 16V X5R 402	DP_INT_AUXCH_N OUT 21 44 48

Misc Ethernet Aliases

26 OUT	ENET_LOW_PWR	TP_ENET_LOW_PWR (MAKE_BASE=TRUE)

Misc FireWire Aliases

28 IN	FW_PME_L	TP_FW_WAKE_L (MAKE_BASE=TRUE)

T29 NOCONNECTS DUE TO SINGLE PORT AND NO DPOUT

42 7 IN	DP_A_PWRDWN	NC_DP_A_PWRDWN (MAKE_BASE=TRUE NO_TEST=TRUE)
42 34 OUT	PM_DPO_EN	R908 4.7K 5% 1/16W MF-LF 402

INTERNAL DP PANEL SOURCE MUX BYPASS

23 IN	DP_T29SRCA_ML_C_P<0>	DP_INT_ML_C_P<0> (MAKE_BASE=TRUE)	OUT 7 44
23 IN	DP_T29SRCA_ML_C_N<0>	DP_INT_ML_C_N<0> (MAKE_BASE=TRUE)	OUT 7 44
23 IN	DP_T29SRCA_ML_C_P<1>	DP_INT_ML_C_P<1> (MAKE_BASE=TRUE)	OUT 7 44
23 IN	DP_T29SRCA_ML_C_N<1>	DP_INT_ML_C_N<1> (MAKE_BASE=TRUE)	OUT 7 44
23 IN	DP_T29SRCA_ML_C_P<2>	DP_INT_ML_C_P<2> (MAKE_BASE=TRUE)	OUT 7 44
23 IN	DP_T29SRCA_ML_C_N<2>	DP_INT_ML_C_N<2> (MAKE_BASE=TRUE)	OUT 7 44
23 IN	DP_T29SRCA_ML_C_P<3>	DP_INT_ML_C_P<3> (MAKE_BASE=TRUE)	OUT 7 44
23 IN	DP_T29SRCA_ML_C_N<3>	DP_INT_ML_C_N<3> (MAKE_BASE=TRUE)	OUT 7 44
23 BI	DP_T29SRCA_AUXCH_C_P	DP_INT_AUXCH_C_P (MAKE_BASE=TRUE)	BI 7 44
23 BI	DP_T29SRCA_AUXCH_C_N	DP_INT_AUXCH_C_N (MAKE_BASE=TRUE)	BI 7 44
23 OUT	DP_T29SRCA_HPD	DP_INT_HPD (MAKE_BASE=TRUE)	IN 21

MISC T29 ALIAS CONNECTIONS

41 34 IN	T29_LSX_R2P (MAKE_BASE=TRUE)	=T29_LSX_R2P OUT 34
41 34 OUT	T29_LSX_P2R (MAKE_BASE=TRUE)	=T29_LSX_P2R IN 34
	TP_T29_A_BIAS (MAKE_BASE=TRUE)	T29_A_BIAS IN 42
43 6 IN	=PP3V3_S4_DPAPWRSW	R909 0 5% 1/16W MF-LF 402 → DPAPWRSW_EN (MAKE_BASE=TRUE) → =DPAPWRSW_EN OUT 43

U5000 IS SLAVE MCU - U9330 IS MASTER
(SEE REFERENCE DESIGN)

=TCMCU_ADDR OUT 34

CLOCKS

22 IN	PCIE_CLK100M_PCIBR_P	PCIE_CLK100M_USB_P (MAKE_BASE=TRUE)	OUT 32 46
22 IN	PCIE_CLK100M_PCIBR_N	PCIE_CLK100M_USB_N (MAKE_BASE=TRUE)	OUT 32 46
22 7 OUT	PCIBR_CLKREQ_L	PCIE_CLKREQ4 (MAKE_BASE=TRUE)	
22 IN	PCIE_CLK100M_T29S_P	NC_PCIE_CLK100M_SRC6P (MAKE_BASE=TRUE NO_TEST=TRUE)	
22 IN	PCIE_CLK100M_T29S_N	NC_PCIE_CLK100M_SRC6N (MAKE_BASE=TRUE NO_TEST=TRUE)	
22 OUT	T29S_CLKREQ_L	PCIE_CLKREQ6 (MAKE_BASE=TRUE)	
22 IN	PCIE_CLK100M_SLOT_P	NC_PCIE_CLK100M_SRC1P (MAKE_BASE=TRUE NO_TEST=TRUE)	
22 IN	PCIE_CLK100M_SLOT_N	NC_PCIE_CLK100M_SRC1N (MAKE_BASE=TRUE NO_TEST=TRUE)	
22 OUT	PCIESLOT_CLKREQ_L	PCIE_CLKREQ1 (MAKE_BASE=TRUE)	
22 IN	PCIE_CLK100M_SATA_P	NC_PCIE_CLK100M_SRC9P (MAKE_BASE=TRUE NO_TEST=TRUE)	
22 IN	PCIE_CLK100M_SATA_N	NC_PCIE_CLK100M_SRC9N (MAKE_BASE=TRUE NO_TEST=TRUE)	
22 OUT	SATA_CLKREQ_L	PCIE_CLKREQ9 (MAKE_BASE=TRUE)	
22 IN	FW_CLK24P576M	NC_FW_CLK24P576M (MAKE_BASE=TRUE NO_TEST=TRUE)	
22 IN	PS161_CLK27M_R	NC_CLK27M (MAKE_BASE=TRUE NO_TEST=TRUE)	
22 IN	PCI_CLK33M_PCIBR	NC_PCI0_CLK33M (MAKE_BASE=TRUE NO_TEST=TRUE)	
22 IN	PCI_CLK33M_NECUSB	NC_PCI2_CLK33M (MAKE_BASE=TRUE NO_TEST=TRUE)	

PCIE CLKREQ ENABLING

22 7 IN	PCIBR_CLKREQ_L (MAKE_BASE=TRUE)	R902 0 5% 1/16W MF-LF 402
22 IN	T29_CLKREQ_L (MAKE_BASE=TRUE)	R903 0 5% 1/16W MF-LF 402

UNUSED T29S GREENCLK

R990 0 5% 1/16W MF-LF 402 → =PPVDDIO_S0_T29S_CLK OUT 22
PPVDDIO_S0_T29S_CLK (MAKE_BASE=TRUE)

22 IN SYSCLK_CLK25M_T29S — NC_SYSCLK_CLK25M_T29S (MAKE_BASE=TRUE NO_TEST=TRUE)

INTERNAL DP PANEL SOURCE MUX BYPASS

23 IN	DP_T29SRCA_ML_C_P<0>	DP_INT_ML_C_P<0> (MAKE_BASE=TRUE)	OUT 7 44
23 IN	DP_T29SRCA_ML_C_N<0>	DP_INT_ML_C_N<0> (MAKE_BASE=TRUE)	OUT 7 44
23 IN	DP_T29SRCA_ML_C_P<1>	DP_INT_ML_C_P<1> (MAKE_BASE=TRUE)	OUT 7 44
23 IN	DP_T29SRCA_ML_C_N<1>	DP_INT_ML_C_N<1> (MAKE_BASE=TRUE)	OUT 7 44
23 IN	DP_T29SRCA_ML_C_P<2>	DP_INT_ML_C_P<2> (MAKE_BASE=TRUE)	OUT 7 44
23 IN	DP_T29SRCA_ML_C_N<2>	DP_INT_ML_C_N<2> (MAKE_BASE=TRUE)	OUT 7 44
23 IN	DP_T29SRCA_ML_C_P<3>	DP_INT_ML_C_P<3> (MAKE_BASE=TRUE)	OUT 7 44
23 IN	DP_T29SRCA_ML_C_N<3>	DP_INT_ML_C_N<3> (MAKE_BASE=TRUE)	OUT 7 44
23 BI	DP_T29SRCA_AUXCH_C_P	DP_INT_AUXCH_C_P (MAKE_BASE=TRUE)	BI 7 44
23 BI	DP_T29SRCA_AUXCH_C_N	DP_INT_AUXCH_C_N (MAKE_BASE=TRUE)	BI 7 44
23 OUT	DP_T29SRCA_HPD	DP_INT_HPD (MAKE_BASE=TRUE)	IN 21

Power-Up Reset Generation

6 =PP3V3_S4_DEVRESET
6 =PP3V3_S0_DEVRESET

Q0910.3 POWERED BY S4 TO ENSURE no glitch when S0 powers-up.

R913 100K 5% 1/16W MF-LF 402
S0_RESET_L (MAKE_BASE=TRUE) — I330 — T29_RESET_L OUT 23
R912 470K 5% 1/16W MF-LF 402
R910 100K 5% 1/16W MF-LF 402
S0_RESET
Q910 DMB53D0UV SOT-563
DEVRESET_P3V3_RC 100ms delay
C910 1UF 10% 6.3V CERM 402

Wake Sources Power State Isolation

ENSURES THAT DEVICES OFF IN S3 DO NOT DRAG DOWN TBLT_WAKE_L.

26 25 =PP3V3_S3_ENET_PHY_FET
R950 100K 5% 1/16W MF-LF 402
Q950 SSM3K15FV SOD-VESM-HF
26 =ENET_WAKE_L IN — ENET_WAKE_L (MAKE_BASE=TRUE)
TBLT_WAKE_L (MAKE_BASE=TRUE) OUT 34 42

35 32 6 =PP3V3_S3_USB
R952 100K 5% 1/16W MF-LF 402
Q952 SSM3K15FV SOD-VESM-HF
32 =USB_WAKE_L IN — USB_WAKE_L (MAKE_BASE=TRUE)

T29 GPIO TO DETECT ERRANT PASSIVE DP CABLE CONNECTION

24 23 11 7 6 =PP3V3_S0_T29P
R900 10K 5% 1/16W MF-LF 402
Q900 SSM3K15FV SOD-VESM-HF
23 T29_GPIO<1> IN
DP_A_PWRDWN OUT 7 42

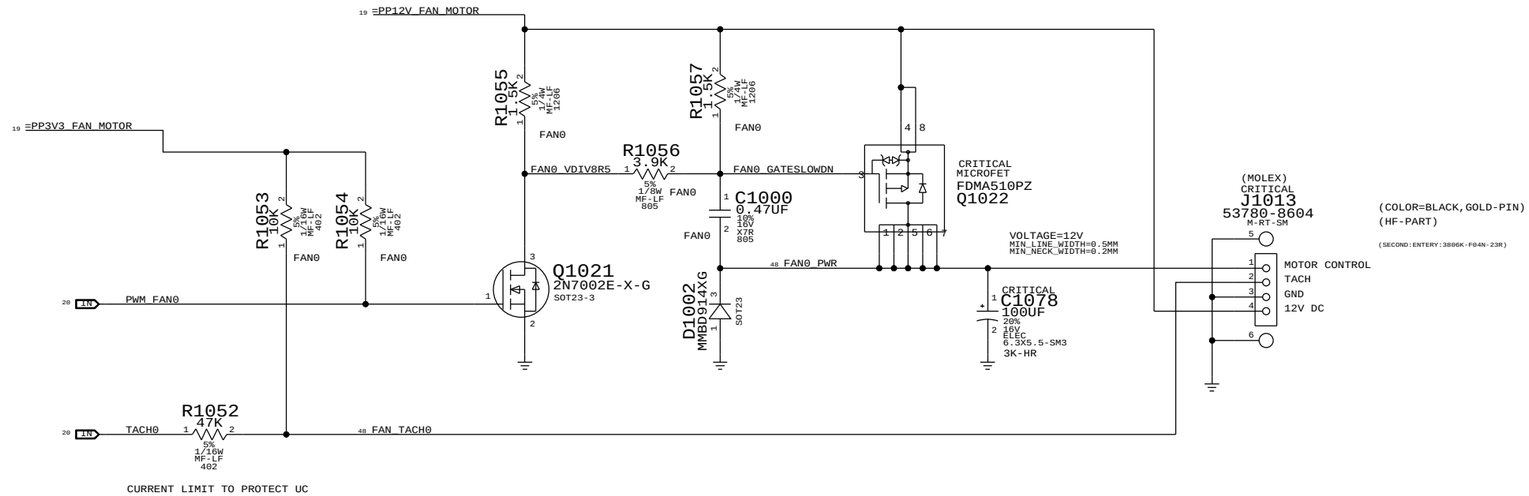
UNUSED T29 ROUTER GPIOS

23 T29_GPIO<2> BI — R901 10K 5% 1/16W MF-LF 402 — =PP3V3_S0_T29P 6 7 11 23 24

SYNC_MASTER=MASTER SYNC_DATE=N/A
PAGE TITLE: Signal Aliases

Apple Inc.

DRAWING NUMBER 051-8774 SIZE D
REVISION C.0.0
BRANCH
PAGE 9 OF 110
SHEET 7 OF 48



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PAGE TITLE: FAN CNTRL & TSENSE

Apple Inc.

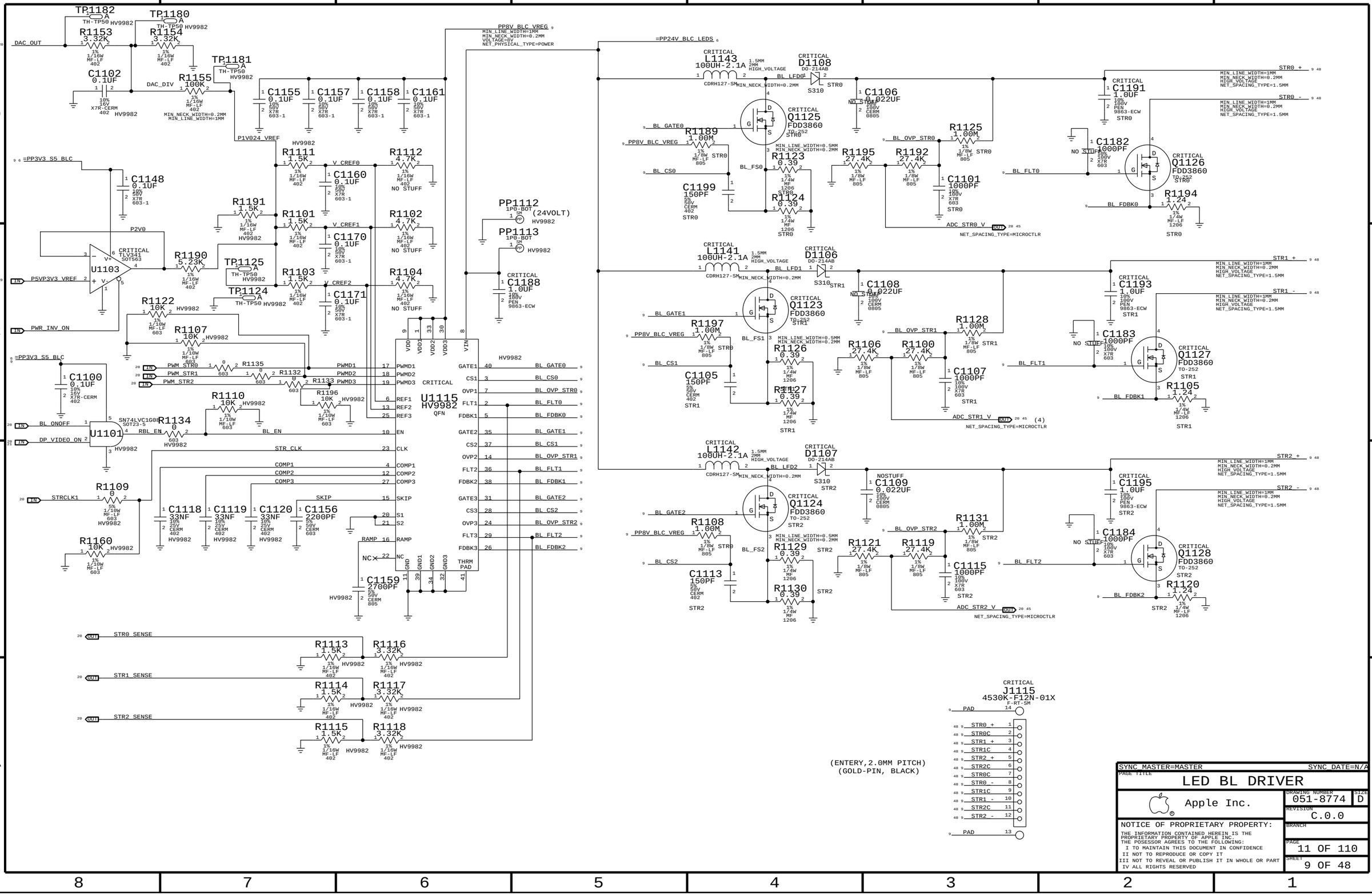
DRAWING NUMBER: 051-8774 SIZE: D

REVISION: C.0.0

BRANCH:

PAGE: 10 OF 110

SHEET: 8 OF 48



SYNC_MASTER=MASTER SYNC_DATE=N/A

PAGE TITLE

LED BL DRIVER

Apple Inc.

DRAWING NUMBER 051-8774 SIZE D

REVISION C.0.0

BRANCH

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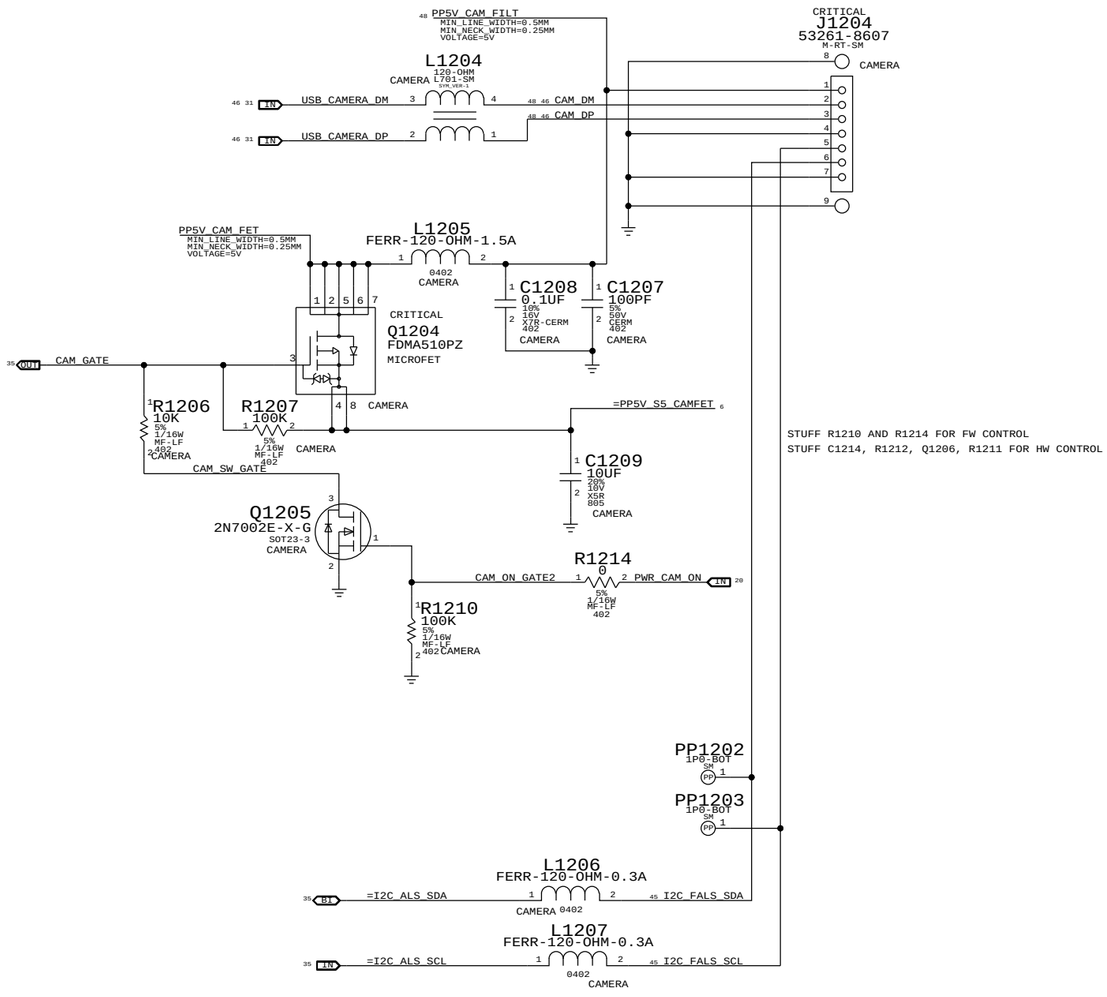
SHEET 9 OF 48



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PAGE TITLE: CAMERA/ALS

Apple Inc.

DRAWING NUMBER: 051-8774 SIZE: D

REVISION: C.0.0

BRANCH:

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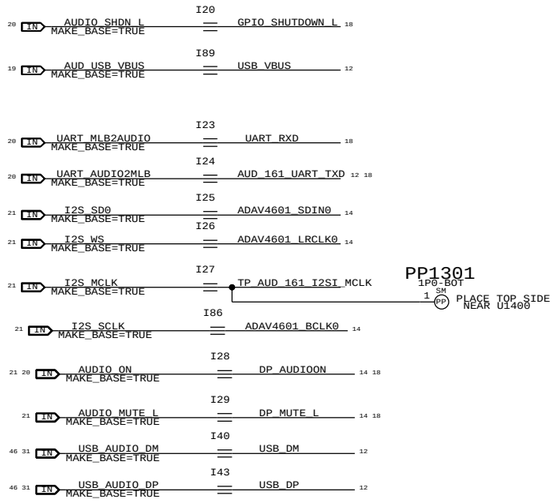
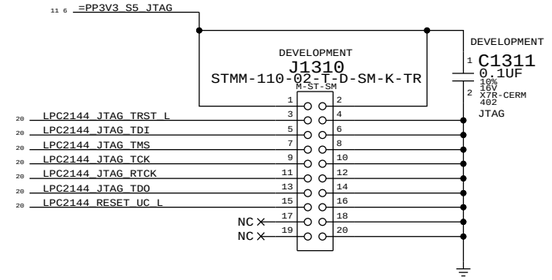
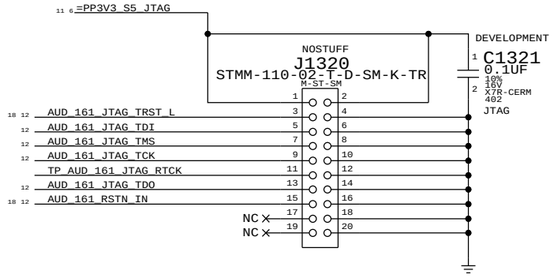
AUDIO ALIASES



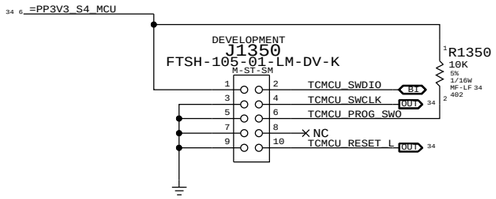
SYSTEM MICRO JTAG

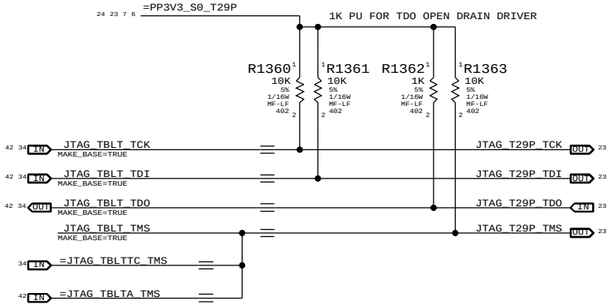


AUDIO JTAG

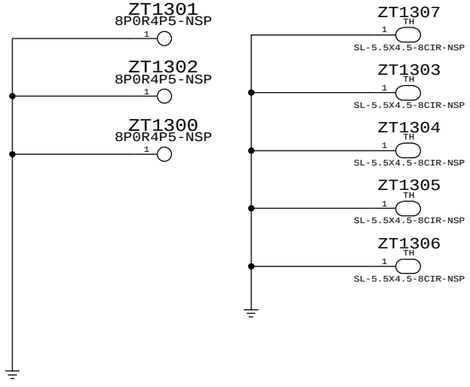


T29 JTAG AND DEBUG

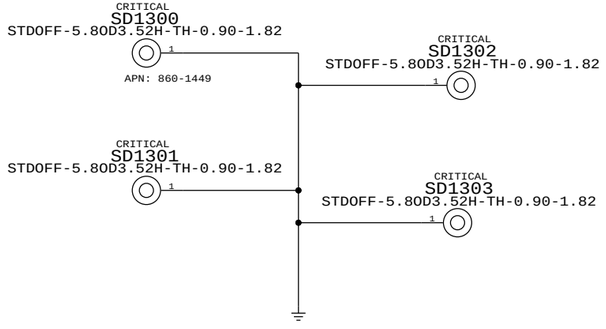




MOUNTING HOLES



J9000 TETHERED CABLE CLAMP STANDOFFS



SYNC_MASTER=K59 SYNC_DATE=08/22/2010

PAGE TITLE
DEBUG, MISC & JTAG

Apple Inc.

DRAWING NUMBER 051-8774 SIZE D
REVISION C.0.0
BRANCH
PAGE 13 OF 110
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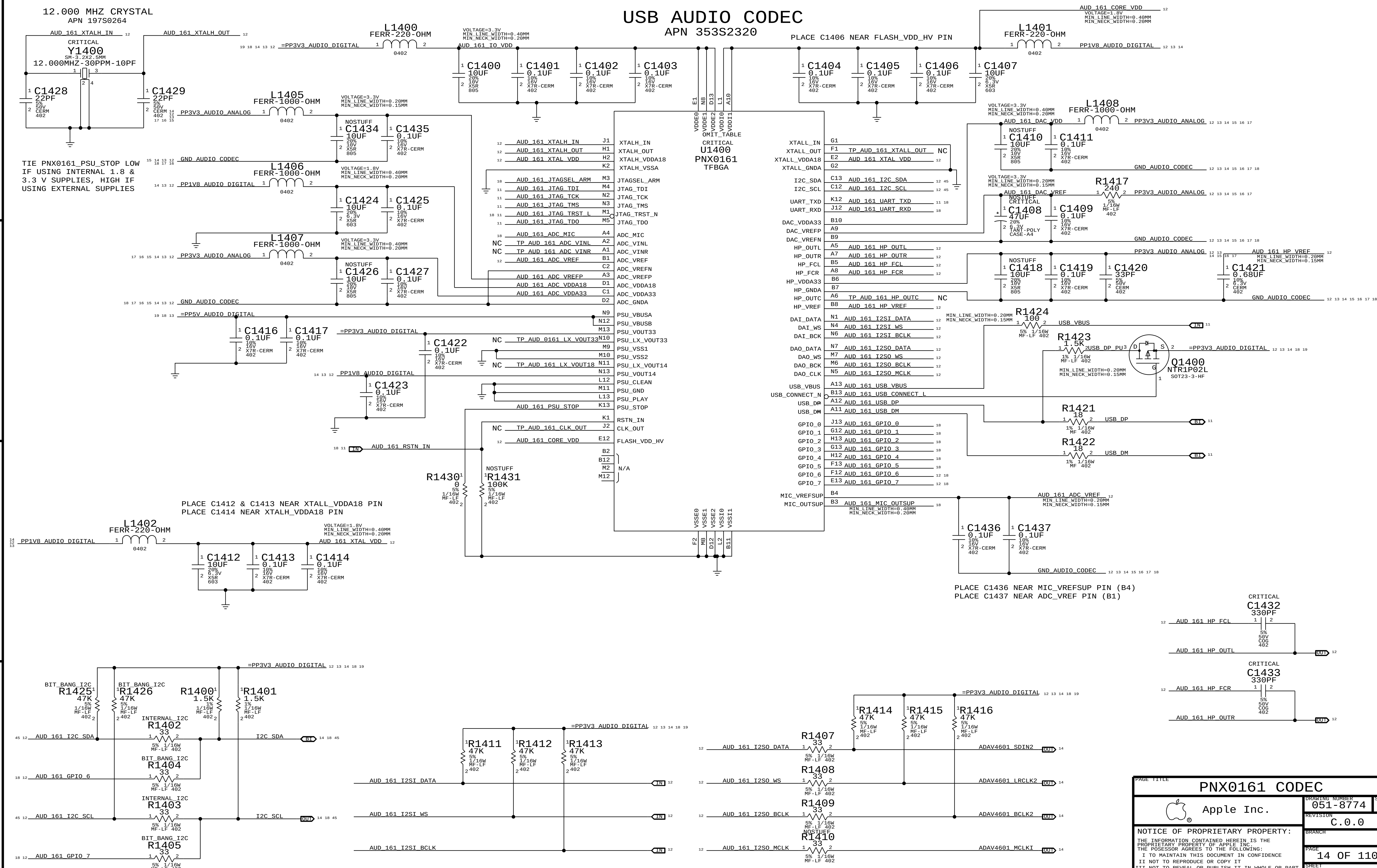
USB AUDIO CODEC

APN 353S2320



PAGE TITLE	PNX0161 CODEC
Apple Inc.	DRAWING NUMBER 051-8774, SIZE D
REVISION	C.0.0
BRANCH	
PAGE	14 OF 110
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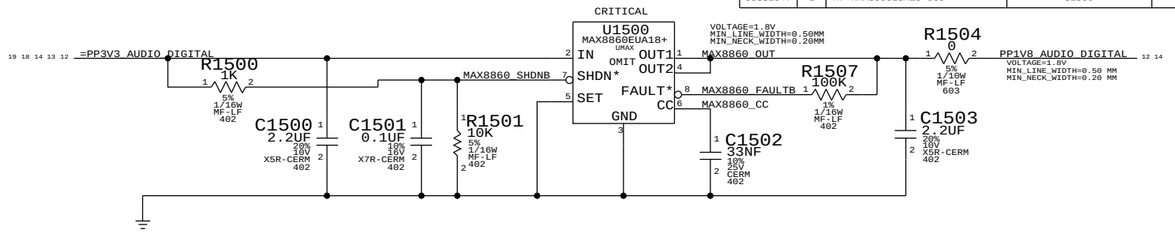
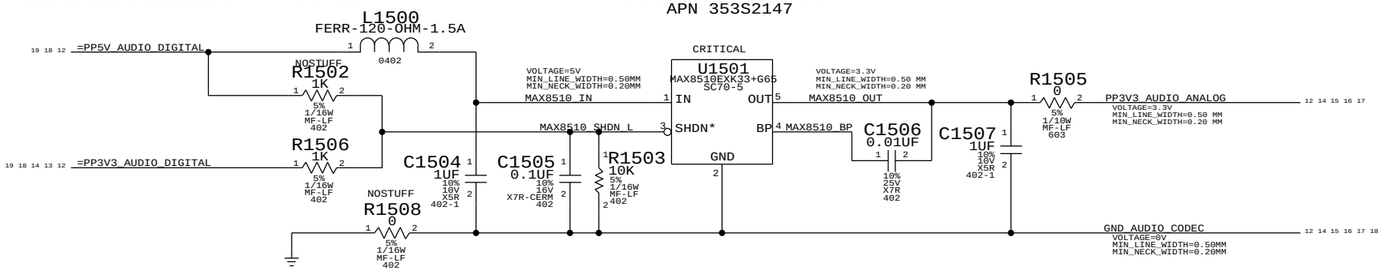
1.8 V REGULATOR
APN 353S2847

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
353S2847	1	HF MAX8860EUA18+G65	U1500	



6/16 IT'S UNCLEAR IF ANALOG 3.3 V NEEDS TO COME UP WITH DIGITAL 3.3 V,
OR IF IT CAN COME UP INDEPENDENTLY (WITH 5.0 V).
ANALOG 3.3 COMES UP WITH DIGITAL 3.3 --> POPULATE R1506
ANALOG 3.3 COMES UP INDEPENDENTLY --> POPULATE R1502

3.3 V REGULATOR
APN 353S2147



PAGE TITLE
AUDIO DC-DC REGULATORS

Apple Inc.

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REVISION C.0.0
BRANCH
PAGE 15 OF 110
SHEET 13 OF 48

AUDIO SIGNAL PROCESSOR
APN 337S3285

PLACE C1601 NEAR PIN 4 (ADC POWER SUPPLY)
PLACE C1602 & C1603 NEAR PINS 58 & 71, RESPECTIVELY (DAC POWER SUPPLIES)
PLACE C1604 & C1605 NEAR PIN 59 (HEADPHONE POWER SUPPLY)
PLACE C1606, C1607, & C1608 NEAR PIN 53 (PLL POWER SUPPLY)

L1600 FERR-220-OHM — PP3V3 AUDIO ANALOG — ADAV4601_AVDD
C1600 10UF 20% 10V X5R 805
C1601 0.1UF 10% 16V X7R-CERM 402
C1602 0.1UF 10% 16V X7R-CERM 402
C1603 0.1UF 10% 16V X7R-CERM 402
NOSTUFF C1604 10UF 20% 10V X5R 805
C1605 0.1UF 10% 16V X7R-CERM 402
C1606 10UF 20% 10V X5R 805
C1607 0.1UF 10% 16V X7R-CERM 402
C1608 1000PF 5% 25V NP0-C0G 402
GND_AUDIO_CODEC

L1601 FERR-220-OHM — ADAV4601_CORE_VDD — PP1V8_AUDIO_DIGITAL
C1609 0.1UF 10% 16V X7R-CERM 402
C1610 0.1UF 10% 16V X7R-CERM 402
C1611 0.1UF 10% 16V X7R-CERM 402
C1612 0.1UF 10% 16V X7R-CERM 402
C1613 0.1UF 10% 16V X7R-CERM 402
C1614 10UF 20% 6.3V X5R 603

L1602 FERR-220-OHM — ADAV4601_IO_VDD — =PP3V3_AUDIO_DIGITAL
C1615 0.1UF 10% 16V X7R-CERM 402
C1616 10UF 20% 10V X5R 805

PLACE R1604 AS CLOSE AS POSSIBLE TO U1601 PIN 33

NOSTUFF R1604 0 5% 1/16W MF-LF 402 — ADAV4601_MCLKI
CRITICAL C1632 18PF 5% 50V CERM 402
CRITICAL Y1600 24.576M HC49-USMD
CRITICAL C1633 18PF 5% 50V CERM 402

R1606 0 5% 1/16W MF-LF 402 — DP_AUDIOON — DP AUDIO CLOCKS
USB AUDIO CLOCKS

R1600 33 5% 1/16W MF-LF 402 — I2C_SDA
R1601 33 5% 1/16W MF-LF 402 — I2C_SCL
R1603 0 5% 1/16W MF-LF 402 — DP_MUTE_L
R1605 0 5% 1/16W MF-LF 402

U1601 ADAV4601 LQFP

NC	TP_ADAV4601_ADC_INL	78	AUXIN1L
NC	TP_ADAV4601_ADC_INR	79	AUXIN1R
	ADAV4601_SDIN3	25	SPDIF_IN0/SDIN3
	ADAV4601_LRCLK0	26	SPDIF_IN1/LRCLK0
	ADAV4601_BCLK0	27	SPDIF_IN2/BCLK0
NO TEST	NC_ADAV4601_LRCLK1	36	SPDIF_IN3/LRCLK1
NO TEST	NC_ADAV4601_BCLK1	35	SPDIF_IN4/BCLK1
	ADAV4601_LRCLK2	18	SPDIF_IN5/LRCLK2
	ADAV4601_BCLK2	19	SPDIF_IN6/BCLK2
	ADAV4601_RESETB	50	RESET*
	ADAV4601_XIN	33	MCLKI/XIN
	TP_ADAV4601_XOUT	34	XOUT
	ADAV4601_I2C_SDA	16	SDA
	ADAV4601_I2C_SCL	17	SCL
NC	TP_ADAV4601_SDO0	37	SDO0/AD0
	ADAV4601_MUTEB	15	MUTE*
DP AUDIO DATA	ADAV4601_SDIN0	22	SDIN0
	ADAV4601_SDIN1	23	SDIN1
USB AUDIO DATA	ADAV4601_SDIN2	24	SDIN2
NC		5,6,7,8,9,10,11,12,60,61,66,74,75,76,77	

		72	AUXOUT1L
		73	AUXOUT1R
		62	AUXOUT3L
		63	AUXOUT3R
		64	AUXOUT4L
		65	AUXOUT4R
NC	TP_ADAV4601_HPOUT1L	57	HPOUT1L
NC	TP_ADAV4601_HPOUT1R	58	HPOUT1R
NC	NC_ADAV4601_PWM1A	42	PWM1A
NC	NC_ADAV4601_PWM1B	43	PWM1B
NC	NC_ADAV4601_PWM2A	44	PWM2A
NC	NC_ADAV4601_PWM2B	45	PWM2B
NC	NC_ADAV4601_PWM3A	46	PWM3A
NC	NC_ADAV4601_PWM3B	47	PWM3B
NC	NC_ADAV4601_PWM4A	48	PWM4A
NC	NC_ADAV4601_PWM4B	49	PWM4B
NC	TP_ADAV4601_PWM_READY	39	PWM_READY
NC	TP_ADAV4601_SDATA_OUT1	38	SPDIF_OUT/SDO1
NC	TP_ADAV4601_MCLK_OUT	30	MCLK_OUT
	ADAV4601_FILTD	67	FILTD
	ADAV4601_FILTA	1	FILTA
	ADAV4601_VREF	2	VREF
	ADAV4601_ISET	80	ISET
	ADAV4601_PLL_LF	54	PLL_LF

AVDD (4, 53, 59, 68, 71) — CRITICAL — DVDD (14, 21, 31, 40, 51) — ODVDD (29)
AGND (3, 55, 56, 69, 70) — DGND (13, 20, 32, 41, 52) — ODGND (28)

ADAV4601_TWTOUT_L, ADAV4601_TWTOUT_R, ADAV4601_WFROUT_L, ADAV4601_WFROUT_R, ADAV4601_SUBOUT_L, TP_ADAV4601_SUBOUT_R → NC

C1617 0.01UF 10% 25V X7R 402
C1618 0.01UF 10% 25V X7R 402
C1619 0.01UF 10% 25V X7R 402
C1620 0.01UF 10% 25V X7R 402
C1621 0.01UF 10% 25V X7R 402
C1622 0.01UF 10% 25V X7R 402
GND_AUDIO_CODEC

R1623 20.0K 1% 1/16W MF-LF 402
C1624 47UF 20% 6.3V TANT-POLY CASE-A4
C1625 0.1UF 10% 16V X7R-CERM 402
NOSTUFF C1626 47UF 20% 6.3V TANT-POLY CASE-A4
C1627 0.1UF 10% 16V X7R-CERM 402
C1628 10UF 20% 6.3V X5R 603
C1629 0.1UF 10% 16V X7R-CERM 402
GND_AUDIO_CODEC

CRITICAL C1630 1000PF 5% 25V NP0-C0G 402
C1631 0.1UF 10% 16V X7R-CERM 402
TP_ADAV4601_PLL_FILT → NC
R1602 2.0K 1% 1/16W MF-LF 402
ADAV4601_AVDD

XW1600 SHORT_L2_SM
NOSTUFF R1607 0 5% 1/16W MF-LF 402
NOSTUFF R1608 0 5% 1/16W MF-LF 402

GND CONNECTIONS WERE ADDED TO ADDRESS EMI CONCERNS ON K59

PAGE TITLE: SIGMA DSP
Apple Inc.
DRAWING NUMBER: 051-8774
SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 16 OF 110
SHEET: 14 OF 48

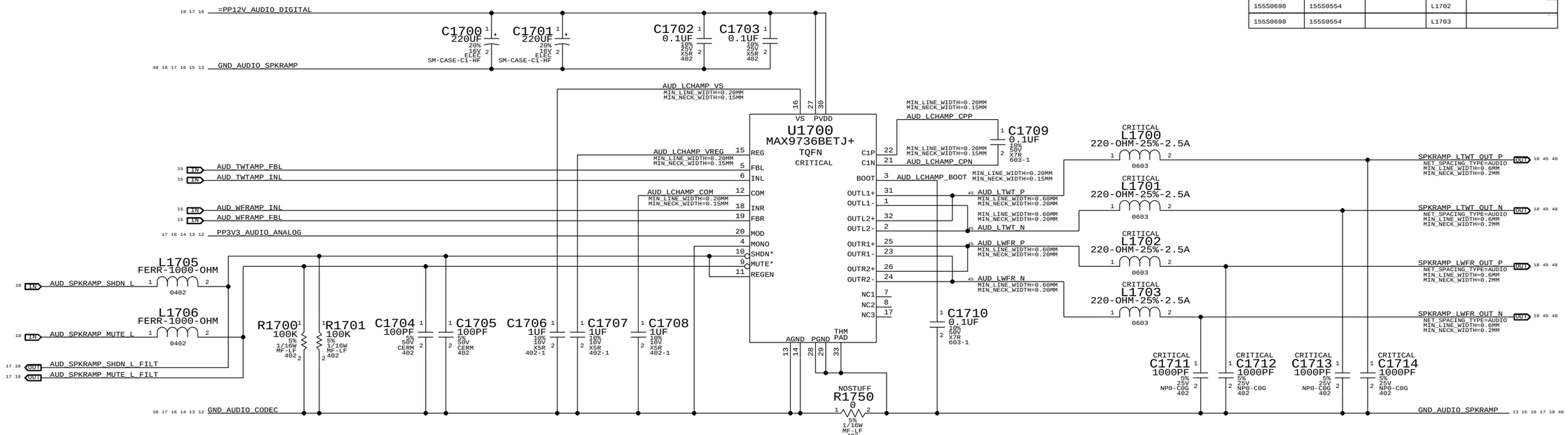
LEFT SPEAKER AMP

APN 353S2042

GAIN = 7.36 V/V (+17.33 DB)

FC = ~774 HZ (TWEETER), ~12 HZ (WOOFER)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0698	155S0554		L1700	
155S0698	155S0554		L1701	
155S0698	155S0554		L1702	
155S0698	155S0554		L1703	



PAGE TITLE: LEFT SPEAKER AMP

Apple Inc.

DRAWING NUMBER: 051-8774 SIZE: D

REVISION: C.0.0

BRANCH:

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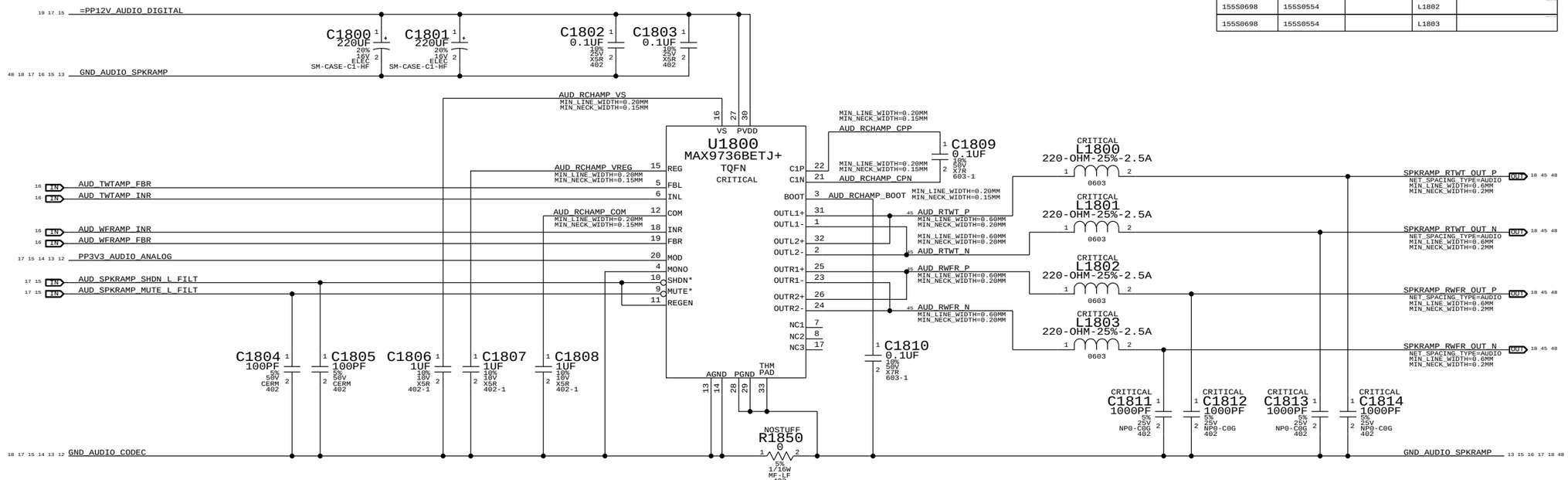
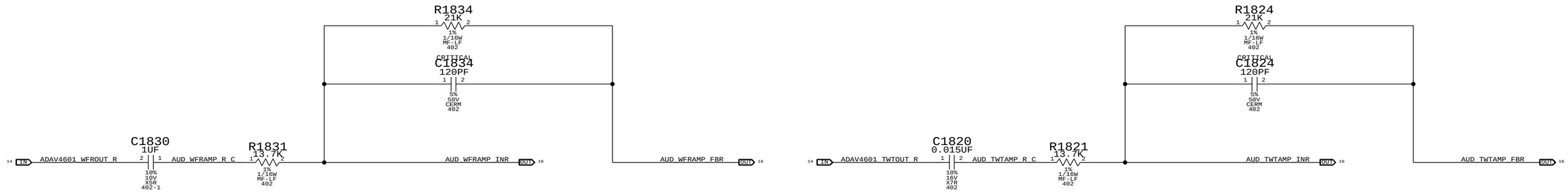
RIGHT SPEAKER AMP

APN 353S2042
GAIN = 7.36 V/V (+17.33 DB)
FC = ~774 HZ (TWEETER), ~12 HZ (WOOFER)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0698	155S0554		L1800	
155S0698	155S0554		L1801	
155S0698	155S0554		L1802	
155S0698	155S0554		L1803	





PAGE TITLE: RIGHT SPEAKER AMP

Apple Inc.

DRAWING NUMBER: 051-8774
SIZE: D
REVISION: C.0.0
BRANCH:
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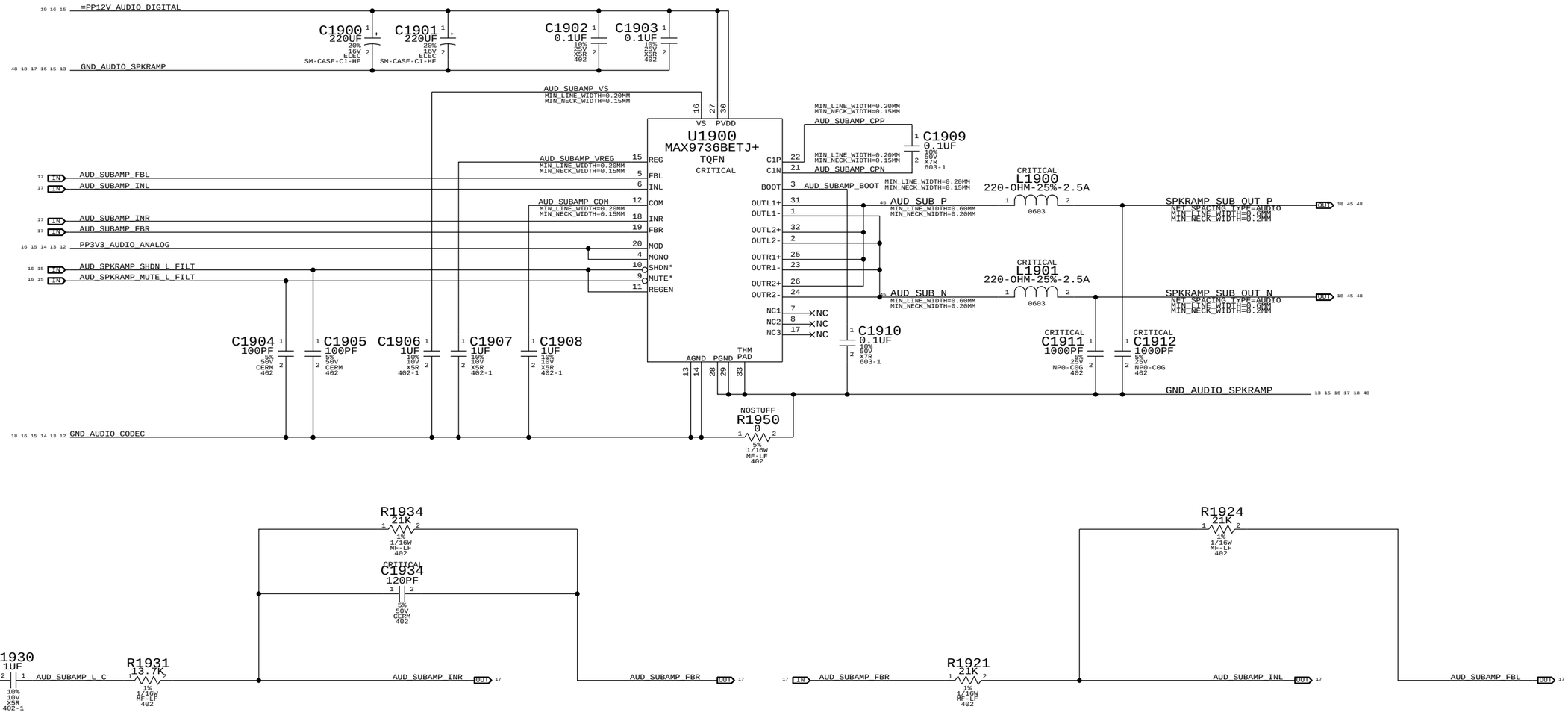
SUBWOOFER SPEAKER AMP

APN 353S2042

GAIN = 7.36 V/V (+17.33 DB)

FC = ~12 HZ

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0698	155S0554		L1900	
155S0698	155S0554		L1901	



PAGE TITLE	SUBWOOFER SPEAKER AMP
	Apple Inc.
DRAWING NUMBER	051-8774
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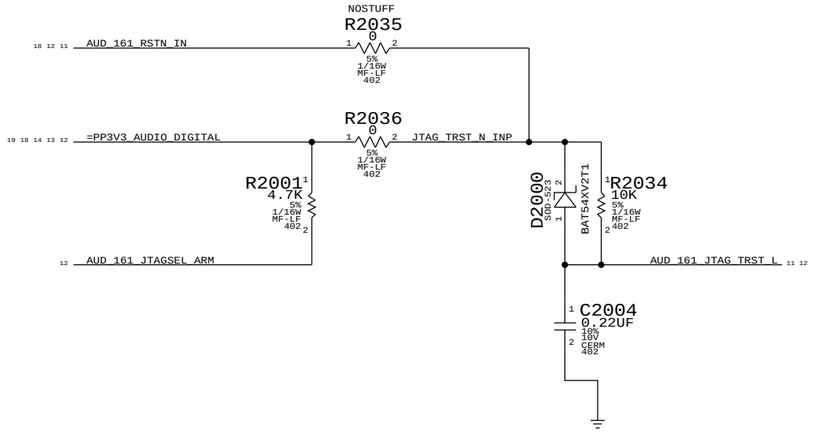
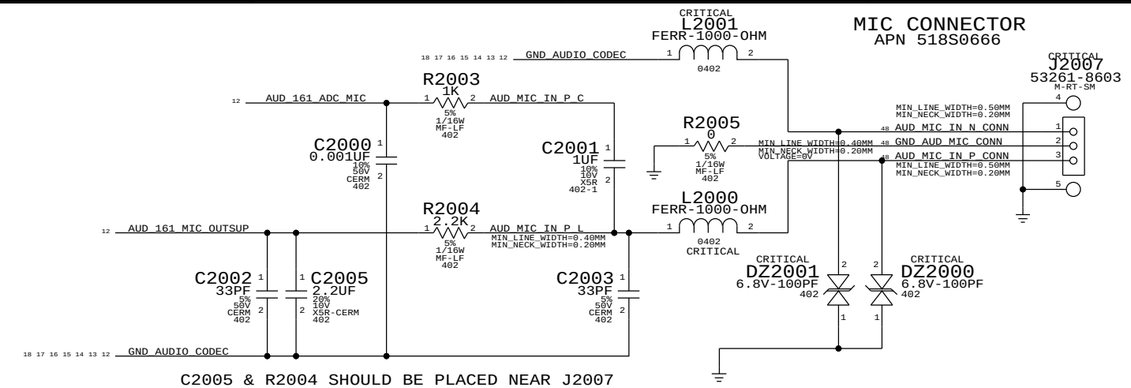
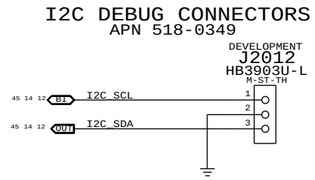
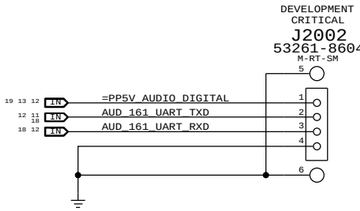


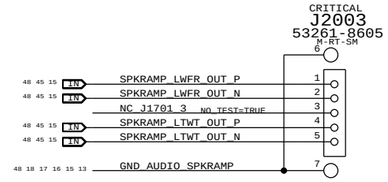


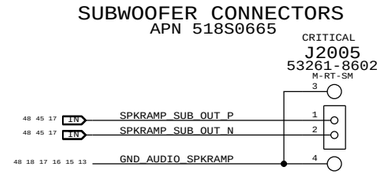
C2005 & R2004 SHOULD BE PLACED NEAR J2007

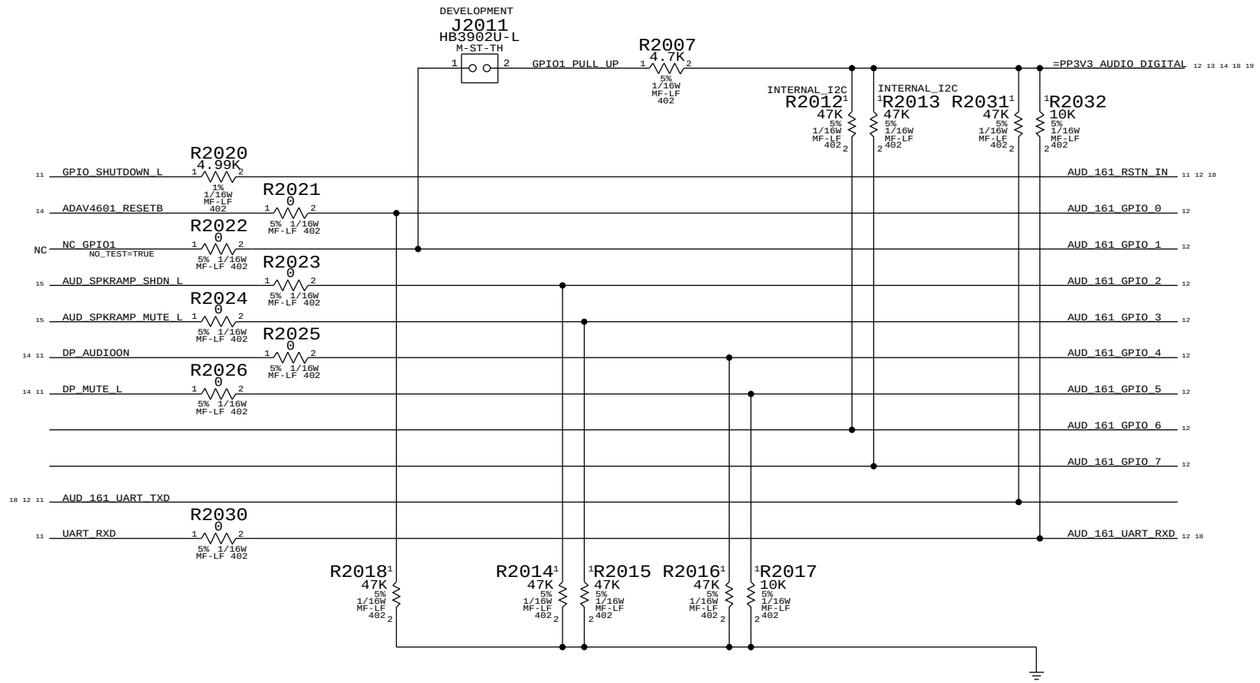


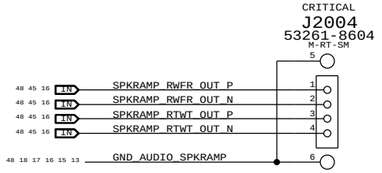
FIXME!!! 3-PIN VERSION NOT RELEASED IN AGILE?
ROW, ROW, ROW YOUR BOAT, GENTLY DOWN THE STREAM.
HA HA, FOOLED YOU, I'M A SUBMARINE.











PAGE TITLE
AUDIO CONNECTORS

Apple Inc.

DRAWING NUMBER 051-8774
SIZE D
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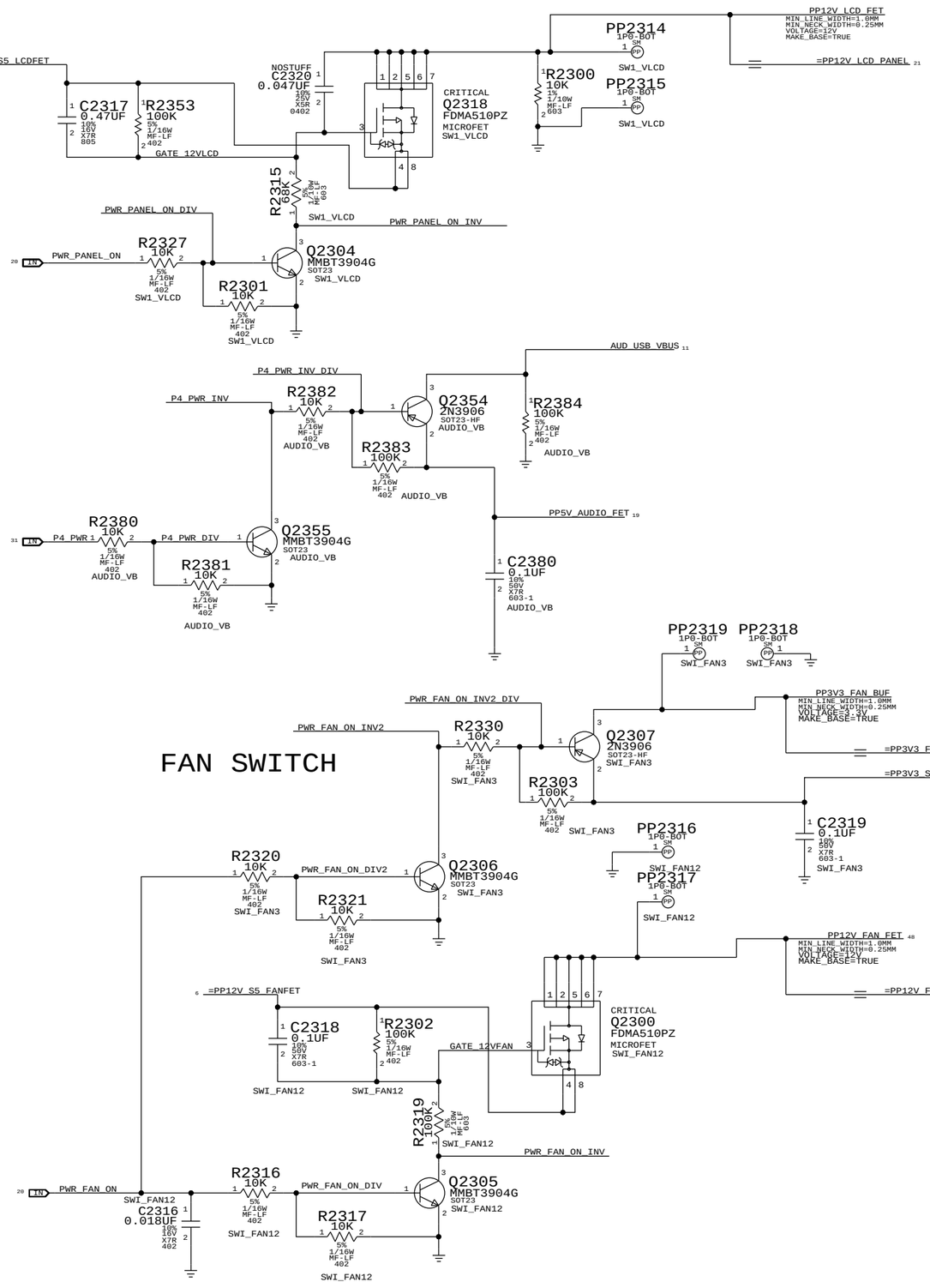
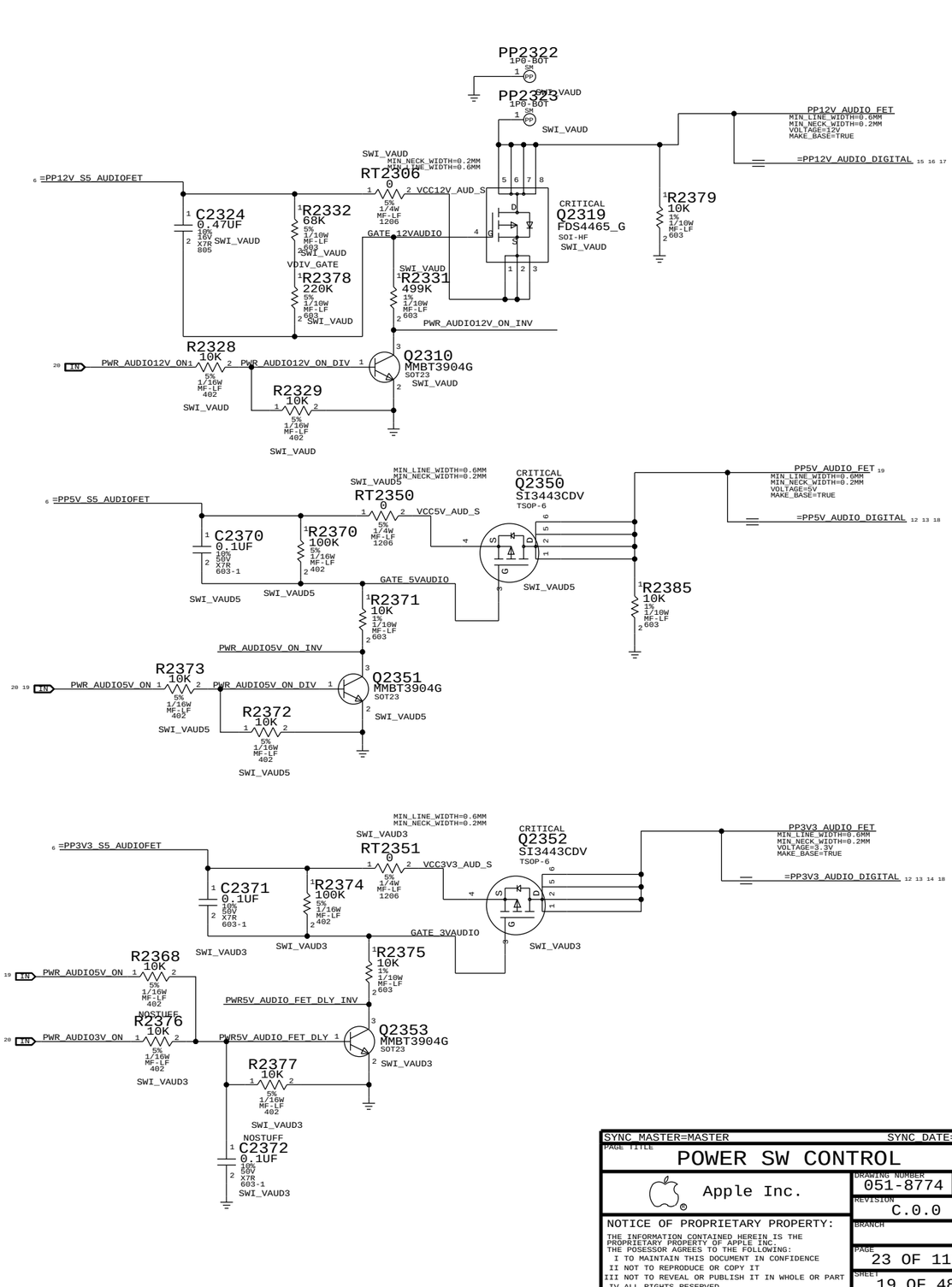
FAN SWITCH





SYNC_MASTER=MASTER SYNC_DATE=N/A

PAGE TITLE: POWER SW CONTROL

Apple Inc.

DRAWING NUMBER: 051-8774 SIZE: D

REVISION: C.0.0

BRANCH:

PAGE: 23 OF 110

SHEET: 19 OF 48

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
311S0394	1	SINGLE NAND GATE SOT553-5	U2608	CRITICAL	

NOTE: NOR GATE FOR OLD SYSTEM UC SLEEP, NAND GATE FOR DEEP SYSTEM UC SLEEP SLEEP
WARNING: DEV CONNECTOR WAKE WILL NO LONGER WORK WITH THIS CONFIGURATION!!!

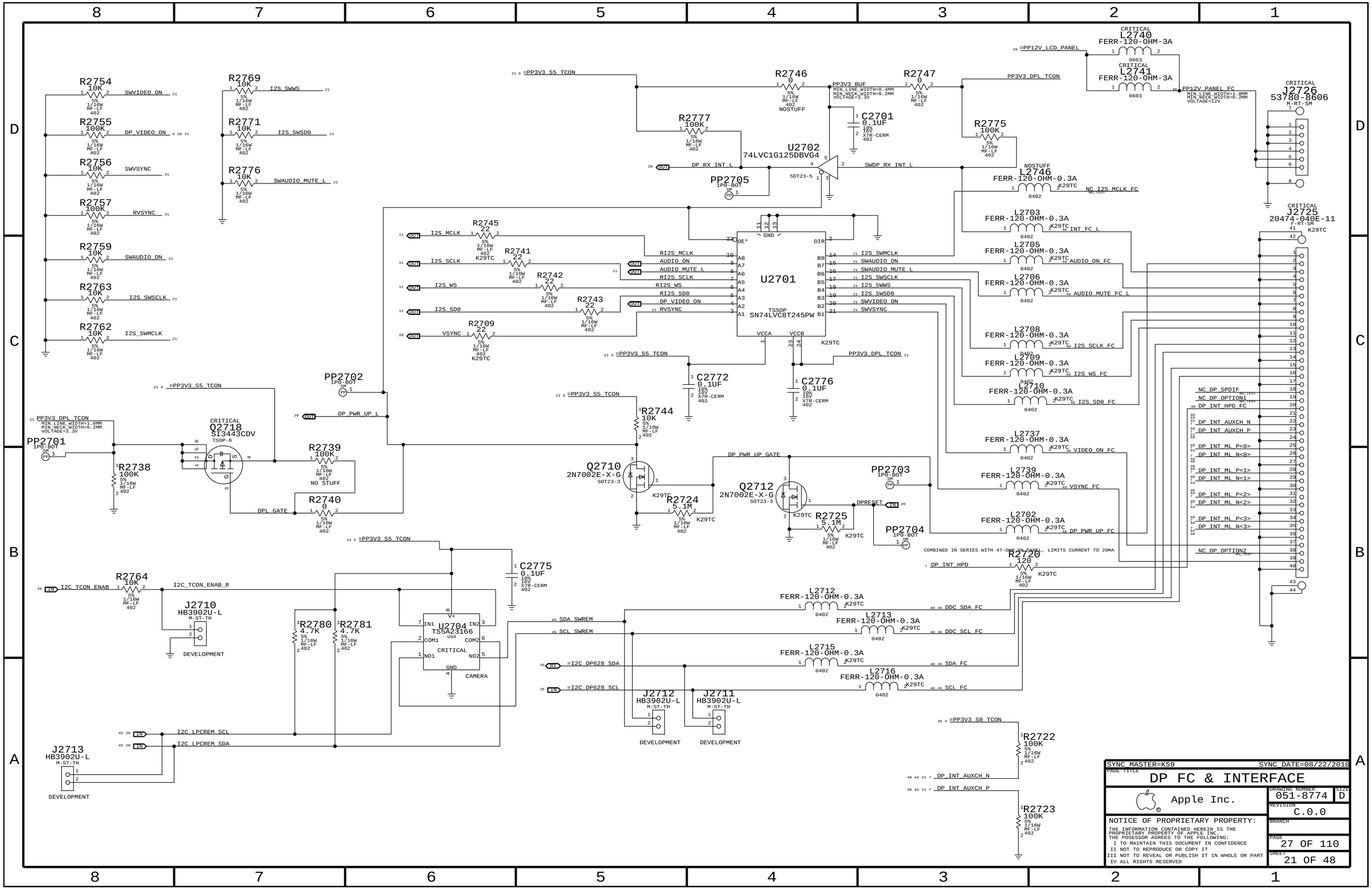
SHORT PINS 2 & 3 FOR JTAG BOOT MODE

SYNC_MASTER=K59 SYNC_DATE=08/22/2010

PAGE TITLE: LPC2144 & PERIPHERALS

Apple Inc.

DRAWING NUMBER: 051-8774 SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 26 OF 110
SHEET: 20 OF 48



SYNC_MASTER=K59 SYNC_DATE=08/22/2010

PAGE TITLE

DP FC & INTERFACE

Apple Inc.

DRAWING NUMBER 051-8774 SIZE D

REVISION C.0.0

BRANCH

PAGE 27 OF 110

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PCI_GEN_SEL	SRC_OUTPUTS
0	Gen 1
1	Gen 2

PCI_SEL	PIN 65
0	24.576MHz
1	33MHz

GCLK_SEL	PIN 5	PIN 6
0	DOT_96+	DOT_96-
1	27M	27M w/SS

FS_C	FS_B	FS_A	CPU MHz
0	0	0	266.6
0	0	1	133.3
0	1	0	200.0
0	1	1	166.6
1	X	X	RSVD

L2860
FERR-120-OHM-1.5A
0402
=PP3V3_S0_CK505
PP3V3_S0_CK505_VDD
MIN_LINE_WIDTH=0.5mm
MIN_NECK_WIDTH=0.2mm
VOLTAGE=3.3V

BYPASS Properties:
U2850.50:53:5 mm
U2850.60:63:5 mm
U2850.67:66:3 mm
U2850.1:3:4 mm
U2850.54:56:4 mm
U2850.4:7:5 mm

C2860 10UF 20% 6.3V X5R 603
C2861 C2862 C2863 C2854 C2855 C2856 0.1UF 10% 16V X5R 402

U2850.11:16:8 mm
U2850.29:32:6 mm
U2850.37:32:8 mm
U2850.44:47:5 mm
=PP1V05_S0_CK505
C2870 C2871 C2872 C2873 0.1UF 10% 16V X5R 402

R2880 R2882 R2884 R2886 R2888 R2890 10K 5% 1/16W MF-LF 402
R2881 R2883 R2885 R2887 R2889 10K 5% 1/16W MF-LF 402
R2891 R2893 10K 5% 1/16W MF-LF 402
R2892 R2894 10K 5% 1/16W MF-LF 402

One 0.1uF per power pin (place at pin).
One 10uF cap per filtered rail.

VDD_CORE VDD_PCI VDD_24 VDD_48 VDD_REF VDD_27 VDD_SRC VDD_CPU
VSS_CORE VSS_PCI VSS_24 VSS_48 VSS_REF VSS_27 VSS_SRC VSS_CPU

CK505_PWRGD
PCIESLOT_CLKREQ_L
T29_CLKREQ_L
PCIBR_CLKREQ_L
ENET_CLKREQ_L
T29S_CLKREQ_L
FW_CLKREQ_L
SATA_CLKREQ_L
CK505_PCI_STOP_L
PCI_CLK33M_PCIBR
CK505_PCIE_GEN2_SEL
CK505_24P576M_L
PCI_CLK33M_NECUSB
CK505_CLK24P576M_FSB
CK505_CLK48M_FSA
CK505_FSC
=I2C_CK505_SCL
=I2C_CK505_SDA
CK505_CLK14M_XTAL_IN
CK505_CLK14M_XTAL_OUT

PCI_CLK33M_PCIBR R2895 33 5% 1/16W MF-LF 402
PCI_CLK33M_NECUSB R2896 33 5% 1/16W MF-LF 402
FW_CLK24P576M R2897 33 5% 1/16W MF-LF 402

U2850
SLG8SP568
QFN
CRITICAL

CKPWRGD/PWRDWN*
CPU_STOP*
CLKREQ_1*
CLKREQ_3*
CLKREQ_4*
CLKREQ_5*
CLKREQ_6*
CLKREQ_8*
CLKREQ_9*
PCI_STOP*
PCIF_0/ITP_EN
PCI_0/PCIE_GEN_SEL (IPD)
PCI_1/PCI_SEL
PCI_2/GCLK_SEL
PCI_3/24.576M/FS_B
48M/FS_A
REF/FS_C
SCL
SDA
XTAL_IN
XTAL_OUT
THRM_PAD

CPU_0 CPU_0* CPU_1 CPU_1* CPU_2_ITP/SRC_10 CPU_2_ITP*/SRC_10* SRC_0 SRC_0* SRC_1 SRC_1* SRC_2 SRC_2* SRC_3 SRC_3* SRC_4 SRC_4* SRC_5 SRC_5* SRC_6 SRC_6* SRC_7 SRC_7* SRC_8 SRC_8* SRC_9 SRC_9* DOT_96/27M DOT_96*/27M_SS

PCIE_CLK100M_SLOT_P
PCIE_CLK100M_SLOT_N
PCIE_CLK100M_T29_P
PCIE_CLK100M_T29_N
PCIE_CLK100M_PCIBR_P
PCIE_CLK100M_PCIBR_N
PCIE_CLK100M_ENET_P
PCIE_CLK100M_ENET_N
PCIE_CLK100M_T29S_P
PCIE_CLK100M_T29S_N
PCIE_CLK100M_FW_P
PCIE_CLK100M_FW_N
PCIE_CLK100M_SATA_P
PCIE_CLK100M_SATA_N
PS161_CLK27M_R

CPU CLKs Unused
Frequency strapped to 133MHz for lowest lowest power. CPU_STOP* must be enabled via I2C to stop CPU_x outputs.
Unused 100MHz (no CLKREQ#)
PCIe x4 Slot 100MHz
Unused 100MHz (no CLKREQ#)
T29 Primary 100MHz
PCI Bridge 100MHz
Caesar-IV PCIe 100MHz
T29 Secondary 100MHz
Unused 100MHz (no CLKREQ#)
FireWire PCIe 100MHz
SATA 100MHz
PS161 27MHz Non-Spread
Unused 27MHz Spread

CRITICAL
Y2850
14.31818
5X3.2-5M
C2850 18pF 5% 50V CERM 402
C2851 18pF 5% 50V CERM 402

NEED TO CHECK CAP VALUE

System 25MHz Clock Generator

GreenClk 25MHz Power
Ethernet XTAL Power
T29S XTAL Power
T29P XTAL Power

=PP3V3_ENET_SYSCLK
=PPVDDIO_ENET_CLK
=PPVDDIO_S0_T29S_CLK
=PPVDDIO_S0_T29P_CLK

C2824 C2822 C2820 0.1UF 20% 10V CERM 402
C2802 1UF 10% 6.3V CERM 402

U2800
SLG3NB146V
TDFN
CRITICAL
VDD VDDIO_A VDDIO_B VDDIO_C
GND THRM PAD
XOUT XIN
25MHZ_A 25MHZ_B 25MHZ_C

SYSCLK_CLK25M_T29S
SYSCLK_CLK25M_ENET
SYSCLK_CLK25M_T29

C2805 12PF 5% 50V CERM 402
C2806 12PF 5% 50V CERM 402
R2805 0 5% 1/16W MF-LF 402
R2806 1M 5% 1/16W MF-LF 402
NO STUFF
CRITICAL
Y2805
25.000MHZ-12PF-20PPM
SM-3.2X2.5MM
NOTE: 30 PPM crystal required

SYSCLK_CLK25M_X2
SYSCLK_CLK25M_X2_R
SYSCLK_CLK25M_X1

SYNC_MASTER=T29_D
SYNC_DATE=03/17/2011
PAGE TITLE: T29 Clocking
Apple Inc.
DRAWING NUMBER: 051-8774
SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 28 OF 110
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CRITICAL
OMIT_TABLE
U3600
T29
FCBGA
(SYM 1 OF 2)

PCIE GEN2

RECEIVE
PER_0_P V19 ← 7 IN PCIE_T29_D2R_P<0>
PER_0_N T19 ← 7 IN PCIE_T29_D2R_N<0>
PER_1_P P19 ← 7 IN PCIE_T29_D2R_P<1>
PER_1_N M19 ← 7 IN PCIE_T29_D2R_N<1>
PER_2_P K19 ← 7 IN PCIE_T29_D2R_P<2>
PER_2_N H19 ← 7 IN PCIE_T29_D2R_N<2>
PER_3_P F19 ← 7 IN PCIE_T29_D2R_P<3>
PER_3_N D19 ← 7 IN PCIE_T29_D2R_N<3>

TRANSMIT
PET_0_P V21 → PCIE_T29_R2D_C_P<0> OUT 7
PET_0_N T21 → PCIE_T29_R2D_C_N<0> OUT 7
PET_1_P P21 → PCIE_T29_R2D_C_P<1> OUT 7
PET_1_N M21 → PCIE_T29_R2D_C_N<1> OUT 7
PET_2_P K21 → PCIE_T29_R2D_C_P<2> OUT 7
PET_2_N H21 → PCIE_T29_R2D_C_N<2> OUT 7
PET_3_P F21 → PCIE_T29_R2D_C_P<3> OUT 7
PET_3_N D21 → PCIE_T29_R2D_C_N<3> OUT 7

TP_T29_MONDC0 — R3610 NO STUFF 0 (5% 1/16W MF-LF 402) — T29_MONDC0 — MONDC0 B21
DEBUG: For monitoring current/voltage
TP_T29_MONDC1 — R3611 NO STUFF 0 (5% 1/16W MF-LF 402) — T29_MONDC1 — MONDC1 A20
TP_T29_MONOBSP — C3615 0.1uF (10% 16V XSR 402) — T29_MONOBSP — MONOBSP K17
DEBUG: For monitoring clock
TP_T29_MONOBSN — C3616 0.1uF (10% 16V XSR 402) — T29_MONOBSN — MONOBSN M17

=PP3V3_S0_T29P 6 7 11 23 24
R3651 10K (5% 1/16W MF-LF 402)

WAKE* F1 ← T29_PCIE_WAKE_L
U3600 not powered in sleep, WAKE# input unusable.
PERST* E6 ← T29_RESET_L IN 7
RSENSE E14 → T29_RSENSE
R3655 1.0K (0.5% 1/16W MF-LF 603)
RBIAS E16 → T29_RBIAS

=PP3V3_S0_T29P 6 7 11 23 24
R3690 3.3K (5% 1/16W MF-LF 402)
R3691 3.3K (5% 1/16W MF-LF 402)
C3690 1UF (10% 6.3V CERM 402)
R3692 3.3K (5% 1/16W MF-LF 402)
R3623 10K (5% 1/16W MF-LF 402)
R3620 10K (5% 1/16W MF-LF 402)
CLKREQ# not functional in endpoint mode.
Pull-ups required on GPIO1 & 2 if unused.

CRITICAL
OMIT_TABLE
U3690
M95160
2Kx8-1.8V
MLP
VCC, VSS, THM PAD
D ← (T29_SPI_MOSI)
C ← T29ROM_WP_L
S_L ← (T29_SPI_CS_L)
W_L ← T29ROM_HOLD_L
HOLD_L
Q → (T29_SPI_MISO)
R3693 3.3K (5% 1/16W MF-LF 402)

MISC

CLK REQUEST
T29_PCIE_CLKREQ_L P3 → PCIE_CLKREQ_0*
T29_GPIO<1> N4 BI 7 → PCIE_CLKREQ_1*
T29_GPIO<2> M3 BI 7 → PCIE_CLKREQ_2*
T29_RSVD L4 → PCIE_CLKREQ_3*

EEPROM
T29_SPI_MOSI 44 P1 → EE_DI
T29_SPI_MISO 44 M1 → EE_DO
T29_SPI_CS_L 44 N2 → EE_CS*
T29_SPI_CLK 44 L2 → EE_CLK

THERM_DP A2 ← T29_THERM_DP

TEST PORT
T29_TEST_EN E4 → TEST_EN
TP_T29_TEST_POINT_0 P5 → TEST_POINT_0
TP_T29_TEST_POINT_1 N6 → TEST_POINT_1
TP_T29_TEST_POINT_2 M5 → TEST_POINT_2
T29_TEST_POINT_3 L6 → TEST_POINT_3

R3625 0 (5% 1/16W MF-LF 402)
R3629 0 (5% 1/16W MF-LF 402)

POWER ON RESET
PCIE_RST_0* K1 → T29_PCIE_RESET_L<0> OUT 7
PCIE_RST_1* J2 → T29_PCIE_RESET_L<1> OUT 7
PCIE_RST_2* K3 → T29_PCIE_RESET_L<2> OUT 7
PCIE_RST_3* J4 → T29_PCIE_RESET_L<3> OUT 7

JTAG
TDI T3 ← JTAG_T29P_TDI IN 11
TMS R4 ← JTAG_T29P_TMS IN 11
TCK R2 ← JTAG_T29P_TCK IN 11
TDO T1 → JTAG_T29P_TDO OUT 11

=PP3V3_S0_T29P 6 7 11 23 24
R3698 10K (5% 1/16W MF-LF 402)

CLOCKS
REFCLK_100_IN_P H17 ← PCIE_CLK100M_T29_P IN 22 44
REFCLK_100_IN_N G16 ← PCIE_CLK100M_T29_N IN 22 44
XTAL_25_IN P17 ← SYSCLK_CLK25M_T29_R
XTAL_25_OUT R16 → TP_T29_XTAL25OUT
TMU_CLK_OUT U2 → T29_TMU_CLK_OUT
TMU_CLK_IN E2 ← T29_TMU_CLK_IN
R3695 806 (1% 1/16W MF-LF 402) — SYSCLK_CLK25M_T29 IN 22
R3696 1K (5% 1/16W MF-LF 402)
NO STUFF
R3699 10K (5% 1/16W MF-LF 402)

DISPLAY

SINK PORT 0
DPSNK0_ML_LANE_3P AA4 ← TP_DP_T29SNK0_MLP<3>
DPSNK0_ML_LANE_3N Y3 ← TP_DP_T29SNK0_MLN<3>
DPSNK0_ML_LANE_2P AA6 ← TP_DP_T29SNK0_MLP<2>
DPSNK0_ML_LANE_2N Y5 ← TP_DP_T29SNK0_MLN<2>
DPSNK0_ML_LANE_1P AA8 ← TP_DP_T29SNK0_MLP<1>
DPSNK0_ML_LANE_1N Y7 ← TP_DP_T29SNK0_MLN<1>
DPSNK0_ML_LANE_0P AA10 ← TP_DP_T29SNK0_MLP<0>
DPSNK0_ML_LANE_0N Y9 ← TP_DP_T29SNK0_MLN<0>
DPSNK0_AUX_CHP V1 ← TP_DP_T29SNK0_AUXCHP
DPSNK0_AUX_CHN W2 ← TP_DP_T29SNK0_AUXCHN
DPSNK0_HOT_PLUG_DET V5 ← TP_DP_T29SNK0_HPD

SINK PORT 1
NC V9 DPSNK1_ML_LANE_3P
NC U8 DPSNK1_ML_LANE_3N
NC V11 DPSNK1_ML_LANE_2P
NC U10 DPSNK1_ML_LANE_2N
NC V13 DPSNK1_ML_LANE_1P
NC U12 DPSNK1_ML_LANE_1N
NC V15 DPSNK1_ML_LANE_0P
NC U14 DPSNK1_ML_LANE_0N
NC V7 DPSNK1_AUX_CHP
NC U6 DPSNK1_AUX_CHN
NC U4 DPSNK1_HOT_PLUG_DET

SOURCE PORT 0
DPSRC0_ML_LANE_3P AA18 → DP_T29SRCA_ML_C_P<3> OUT 7
DPSRC0_ML_LANE_3N Y17 → DP_T29SRCA_ML_C_N<3> OUT 7
DPSRC0_ML_LANE_2P AA16 → DP_T29SRCA_ML_C_P<2> OUT 7
DPSRC0_ML_LANE_2N Y15 → DP_T29SRCA_ML_C_N<2> OUT 7
DPSRC0_ML_LANE_1P AA14 → DP_T29SRCA_ML_C_P<1> OUT 7
DPSRC0_ML_LANE_1N Y13 → DP_T29SRCA_ML_C_N<1> OUT 7
DPSRC0_ML_LANE_0P AA12 → DP_T29SRCA_ML_C_P<0> OUT 7
DPSRC0_ML_LANE_0N Y11 → DP_T29SRCA_ML_C_N<0> OUT 7
DPSRC0_AUX_CHP W16 → DP_T29SRCA_AUXCH_C_P BI 7
DPSRC0_AUX_CHN U16 → DP_T29SRCA_AUXCH_C_N BI 7
DPSRC0_HOT_PLUG_DET V3 → DP_T29SRCA_HPD IN 7

DP_ATEST Y19 ← T29_DP_ATEST
DP_RES_0 Y21
DP_RES_1 AA20 ← T29_DP_RES
R3685 14.0K (1% 1/16W MF-LF 402)
R3632 100K (5% 1/16W MF-LF 402)

100pF SRF > 40MHz
BYPASS=U3600.Y19::2mm
BYPASS=U3600.Y19::5.08mm
C3685 100PF (5% 50V CERM 402)
C3686 0.01UF (10% 50V X7R 402)

PORTS

CABLE PORT - LINK 0
T29_R2C_C_P<0> A6 → PRT0_T29T_P OUT 41 44
T29_R2C_C_N<0> A4 → PRT0_T29T_N OUT 41 44
T29_C2R_P<0> C4 ← PRT0_T29R_P IN 41 44
T29_C2R_N<0> C2 ← PRT0_T29R_N IN 41 44
T29_R2C_LSEO<0> J6 → T29_0_LSEO OUT 23
T29_C2R_LSEO<0> K5 ← T29_0_LSEO IN 23
PORT0

CABLE PORT - LINK 1
T29_R2C_C_P<1> A10 → PRT1_T29T_P OUT 41 44
T29_R2C_C_N<1> A8 → PRT1_T29T_N OUT 41 44
T29_C2R_P<1> C8 ← PRT1_T29R_P IN 41 44
T29_C2R_N<1> C6 ← PRT1_T29R_N IN 41 44
T29_R2C_LSEO<1> G6 → T29_1_LSEO OUT 34
T29_C2R_LSEO<1> H5 ← T29_1_LSEO IN 34
PORT1

I2C_T29_SDA F3 ← T29_SDA BI 35 44
I2C_T29_SCL F5 ← T29_SCL OUT 35 44

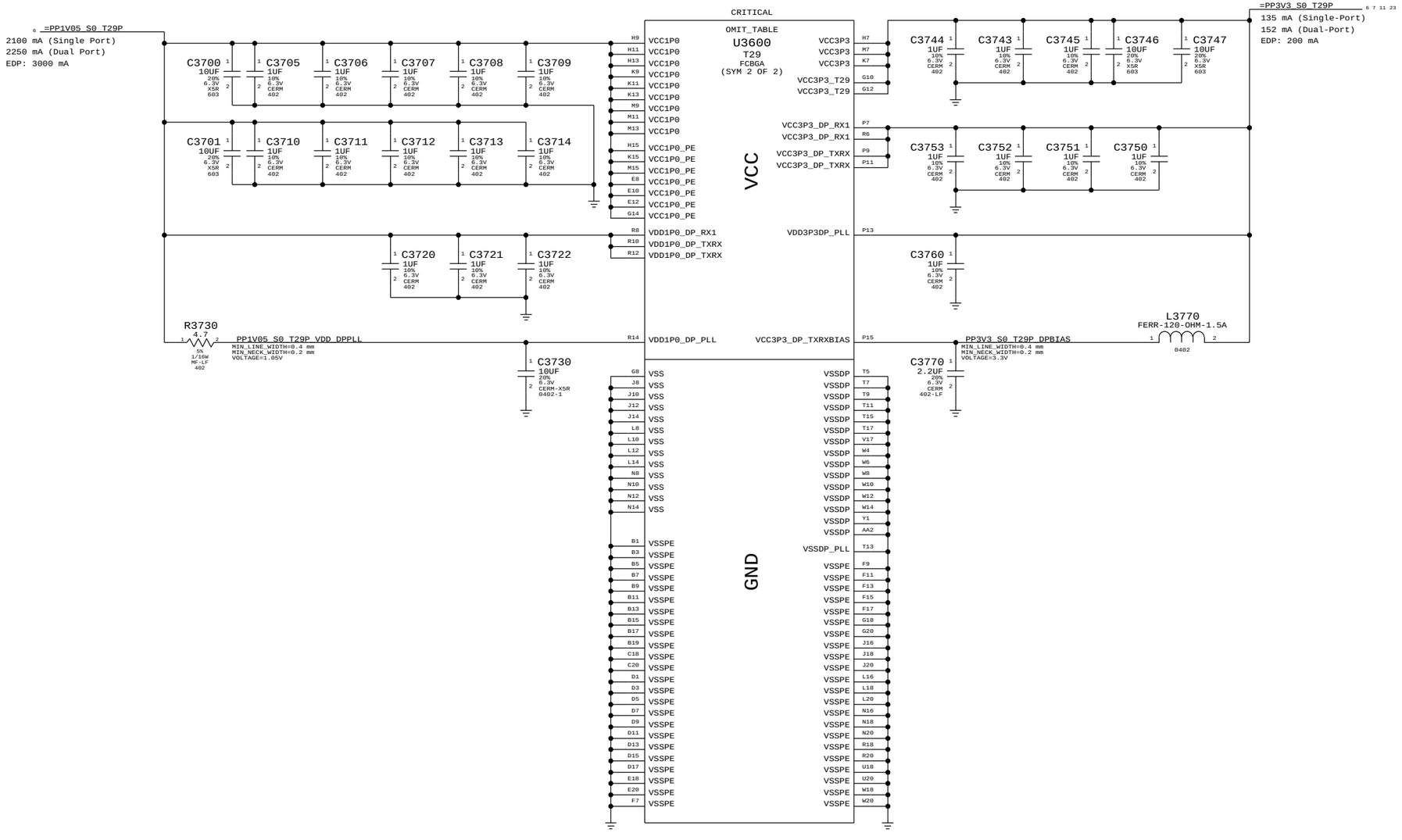
PORT2
MDP PORT A - LINK 0
PRT2_T29T_P A14 → T29_R2D_C_P<0> OUT 42 44
PRT2_T29T_N A12 → T29_R2D_C_N<0> OUT 42 44
PRT2_T29R_P C12 ← T29_D2R_P<0> IN 42 44
PRT2_T29R_N C10 ← T29_D2R_N<0> IN 42 44
T29_2_LSEO G4 → T29_LSEO<0> OUT 23
T29_2_LSOE H3 ← T29_LSOE<0> IN 23

PORT3
MDP PORT A - LINK 1
PRT3_T29T_P A18 → T29_R2D_C_P<1> OUT 42 44
PRT3_T29T_N A16 → T29_R2D_C_N<1> OUT 42 44
PRT3_T29R_P C16 ← T29_D2R_P<1> IN 42 44
PRT3_T29R_N C14 ← T29_D2R_N<1> IN 42 44
T29_3_LSEO G2 → T29_LSEO<1> OUT 42
T29_3_LSOE H1 ← T29_LSOE<1> IN 42

23 T29_R2C_LSEO<0> MAKE_BASE=TRUE = =T29_R2C_LSEO<0> 34
23 T29_C2R_LSEO<0> MAKE_BASE=TRUE = =T29_C2R_LSEO<0> 34
23 T29_LSEO<0> MAKE_BASE=TRUE = =T29_LSEO<0> 42
23 T29_LSOE<0> MAKE_BASE=TRUE = =T29_LSOE<0> 42

NOTE: C2R = Cable to Router
R2C = Router to Cable

SYNC_MASTER=T29_D SYNC_DATE=11/01/2010
PAGE TITLE: T29 Primary (1 of 2)
Apple Inc.
DRAWING NUMBER: 051-8774 SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 36 OF 110
SHEET: 23 OF 48



Current numbers from Vendor slide (<REDACTED> power measure 1.ppt), emailed 6/21/2010, TDP @ 90C.

SYNC_MASTER=T29_D SYNC_DATE=03/17/2011

PAGE TITLE: T29 Primary (2 of 2)

Apple Inc.

DRAWING NUMBER: 051-8774 SIZE: D

REVISION: C.0.0

BRANCH:

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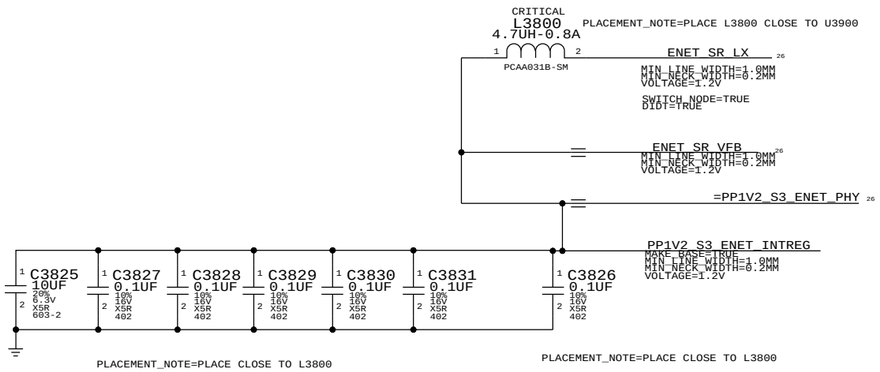
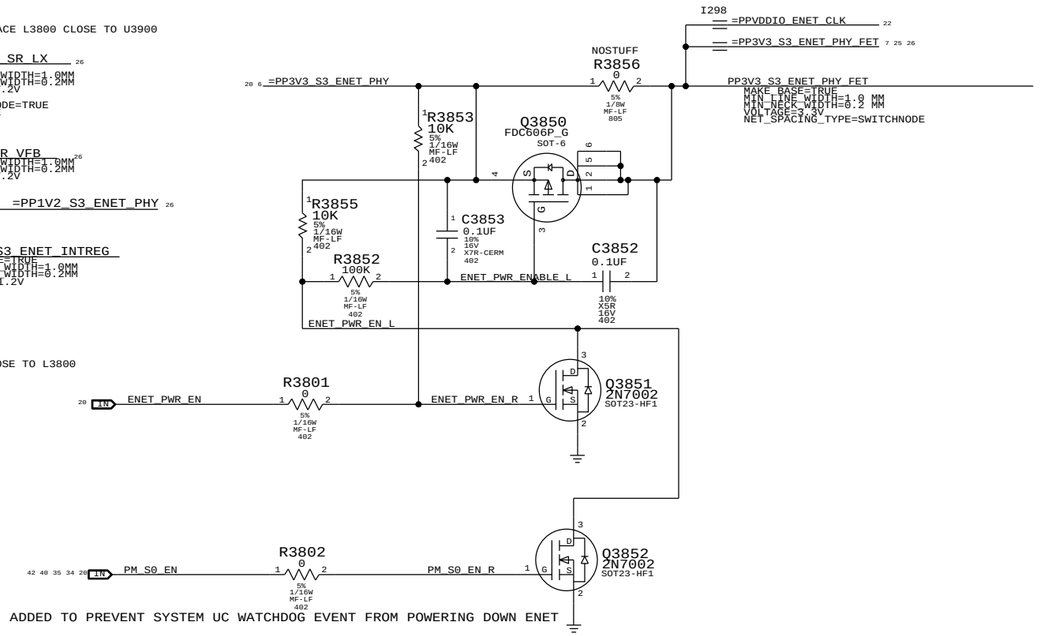
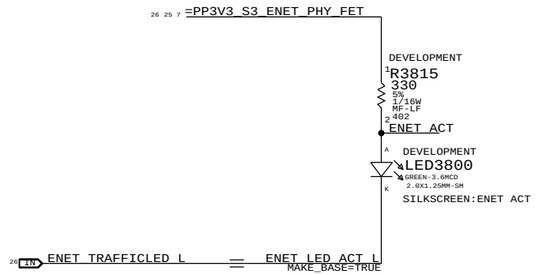
CAESAR IV 1.2V INT.VR CMPTS

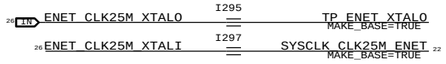


CAESAR IV POWER ENABLE CIRCUIT



CAESAR IV ACTIVITY LED





SYNC_MASTER=K62 SYNC_DATE=09/16/2010

PAGE TITLE
CAESAR IV SUPPORT

Apple Inc.

DRAWING NUMBER 051-8774 SIZE D
REVISION C.0.0
BRANCH
PAGE 38 OF 110
SHEET 25 OF 48

BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_S3_ENET_PHY.
If enabled: VDD/VDDP connect to =PP3V3_S3_ENET_PHY (add bypassing), LX connects to inductor.
Special Star routing needed on these pins. Decoupling on Pg 37.

281mA (1000base-T max power, Caesar IV)

=PP3V3_S3_ENET_PHY_FET

C3979 4.7UF 20% 6.3V CERM 603

R3901 0 5% 1/16W MF-LF 402

ENET_3V3_S3_SR_IN
SWITCH_NODE=TRUE
DIDT=TRUE
NET_SPACING_TYPE=SWITCHNODE
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V

C3980 0.1UF 10% 16V X5R 402

C3981 0.1UF 10% 16V X5R 402

CRITICAL
L3900 FERR-600-OHM-0.5A SM

PP3V3_S3_ENET_PHY_XTALVDDH
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

C3900 0.1UF 10% 16V X7R-CERM 402

R3900 0 5% 1/16W MF-LF 402

ENET_XTALVDDH
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

CRITICAL
L3905 FERR-600-OHM-0.5A SM

PP3V3_S3_ENET_PHY_BIASVDDH
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

C3905 0.1UF 10% 16V X7R-CERM 402

CRITICAL
L3910 FERR-600-OHM-0.5A SM

PP3V3_S3_ENET_PHY_AVDDH
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

R3910 4.7K 5% 1/16W MF-LF 402

C3910 0.1UF 10% 16V X7R-CERM 402

C3911 0.1UF 10% 16V X7R-CERM 402

R3942 IS A LEAKAGE PATH, SO RESISTOR VALUE IS SMALL.

=PP3V3_S0_ENET_PHY

Current Limiting Resistor

R3942 4.7K 5% 1/16W MF-LF 402

NOSTUFF
R3998 0 5% 1/16W MF-LF 402

ENET_VMAIN_CTRL

R3940 4.7K 5% 1/16W MF-LF 402

R3941 4.7K 5% 1/16W MF-LF 402

C3917 0.1UF 10% 16V X7R-CERM 402

C3918 0.1UF 10% 16V X7R-CERM 402

C3915 4.7UF 10% 6.3V X5R-CERM 603

C3916 0.1UF 10% 16V X7R-CERM 402

ENET_SR_LX

ENET_SR_VFB

Internal 1.2V Switching Regulator pins.

=PP1V2_S3_ENET_PHY
396mA (1000base-T, Caesar II)

CRITICAL
L3920 FERR-600-OHM-0.5A SM

PP1V2_S3_ENET_PHY_AVDDL
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V

C3921 0.1UF 10% 16V X7R-CERM 402

C3920 4.7UF 10% 6.3V X5R-CERM 603

CRITICAL
L3925 FERR-600-OHM-0.5A SM

PP1V2_S3_ENET_PHY_PCIEPLL
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V

C3926 0.1UF 10% 16V X7R-CERM 402

C3925 4.7UF 10% 6.3V X5R-CERM 603

CRITICAL
L3930 FERR-600-OHM-0.5A SM

PP1V2_S3_ENET_PHY_GPHYPLL
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.2V

C3931 0.1UF 10% 16V X7R-CERM 402

C3930 4.7UF 10% 6.3V X5R-CERM 603

C3936 0.1UF 10% 16V X7R-CERM 402

C3935 10UF 10% 6.3V X5R 805

AVDDH, BIASVDDH, XTALVDDH, VDDO, SR_VDD, SR_VDDP, SR_LX, SR_VFB, AVDDL, PCIE_PLLVDDL, GPHY_PLLVDDL, VDDC

OMIT_TABLE

U3900 BCM57761A0KMLG QFN

PCIE_ENET_D2R_N — C3950 0.1uF
PCIE_ENET_D2R_P — C3951 0.1uF
PCIE_ENET_R2D_C_P — C3955 0.1uF
PCIE_ENET_R2D_C_N — C3956 0.1uF

ENET_WAKE:PCIE
R3943 0 5% 1/16W MF-LF 402

=ENET_WAKE_L (See note)

WAKE#

Must isolate from PCIe WAKE# if PHY is powered-down in S3/S5. Standard N-channel FET isolation suggested.
If PHY is always powered then alias =ENET_WAKE_L to PCIE_WAKE_L.

ENET_VMAIN_PRSNT	40	VMAIN_PRSNT (IPD-ENET)
PCIE_ENET_D2R_C_N	16	PCIE_TXD_N
PCIE_ENET_D2R_C_P	17	PCIE_TXD_P
PCIE_ENET_R2D_P	22	PCIE_RXD_P
PCIE_ENET_R2D_N	23	PCIE_RXD_N
PCIE_CLK100M_ENET_P	20	PCIE_REFCLK_P
PCIE_CLK100M_ENET_N	19	PCIE_REFCLK_N
ENET_RESET_L	6	PERST* (IPD)
ENET_CLKREQ_L	7	CLKREQ* (OD)
ENET_WAKE_R_L	1	WAKE* (OD)
ENET_LOW_PWR	2	LOW_PWR (IPD)
ENET_SMB_CLK	4	SMB_CLK
ENET_SMB_DATA	5	SMD_DATA (IPD-ENETM)
ENET_SCLK	46	SCLK/SPD1000LED*
ENET_MISO	44	SI*/EEDATA
ENET_MOSI	45	SO*/LINKLED*
ENET_CS_L	43	CS*/EECLK
TP_ENET_SPD100LED_L	48	SPD100LED* (OD)
ENET_TRAFFICLED_L	47	TRAFFICLED* (OD)
ENET_CLK25M_XTALI	13	XTALI
ENET_CLK25M_XTALO	14	XTALO
ENET_RDAC	26	RDAC

(IPU)

TRD0_P	28	ENETCONN_MDI_P<0>
TRD0_N	29	ENETCONN_MDI_N<0>
TRD1_P	32	ENETCONN_MDI_P<1>
TRD1_N	31	ENETCONN_MDI_N<1>
TRD2_P	34	ENETCONN_MDI_P<2>
TRD2_N	35	ENETCONN_MDI_N<2>
TRD3_P	38	ENETCONN_MDI_P<3>
TRD3_N	37	ENETCONN_MDI_N<3>

GPIO_0 — ENET_WOL_ENABLE

ENET_WAKE:GPIO
R3999 0 5% 1/16W MF-LF 402 — =ENET_WAKE_L

THRM_PAD 49

R3965 1.24K 1% 1/16W MF-LF 402

PHY Non-Volatile Memory

ROM contains MAC address, PCIe config info as well as code for Bonjour proxy.
Avoids need for EFI to program at startup.
(Required ROM size 1 Mbit)

=PP3V3_S3_ENET_PHY_FET

R3993 4.7K 5% 1/16W MF-LF 402

R3992 4.7K 5% 1/16W MF-LF 402

R3904 0 5% 1/16W MF-LF 402

C3990 0.1UF 10% 16V X7R-CERM 402

U3990 M45PE10 SOIC OMIT_TABLE

ENET_SCLK	2	C
ENET_CS_L	4	S*
ENET_SWP_L	5	W*
ENET_SRESET_L	3	RESET*
VCC	8	
VSS	7	
ENET_MOSI	1	D
ENET_MISO	8	Q

NOSTUFF
R3990 4.7K 5% 1/16W MF-LF 402

R3997 4.7K 5% 1/16W MF-LF 402

NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures ENET for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
NOTE: ENETM requires SI pull-down instead of SO.

SYNC_MASTER=TONY SYNC_DATE=10/01/2010

PAGE TITLE: ETHERNET PHY (CAESAR IV)

Apple Inc.

DRAWING NUMBER 051-8774 SIZE D
REVISION C.0.0
BRANCH
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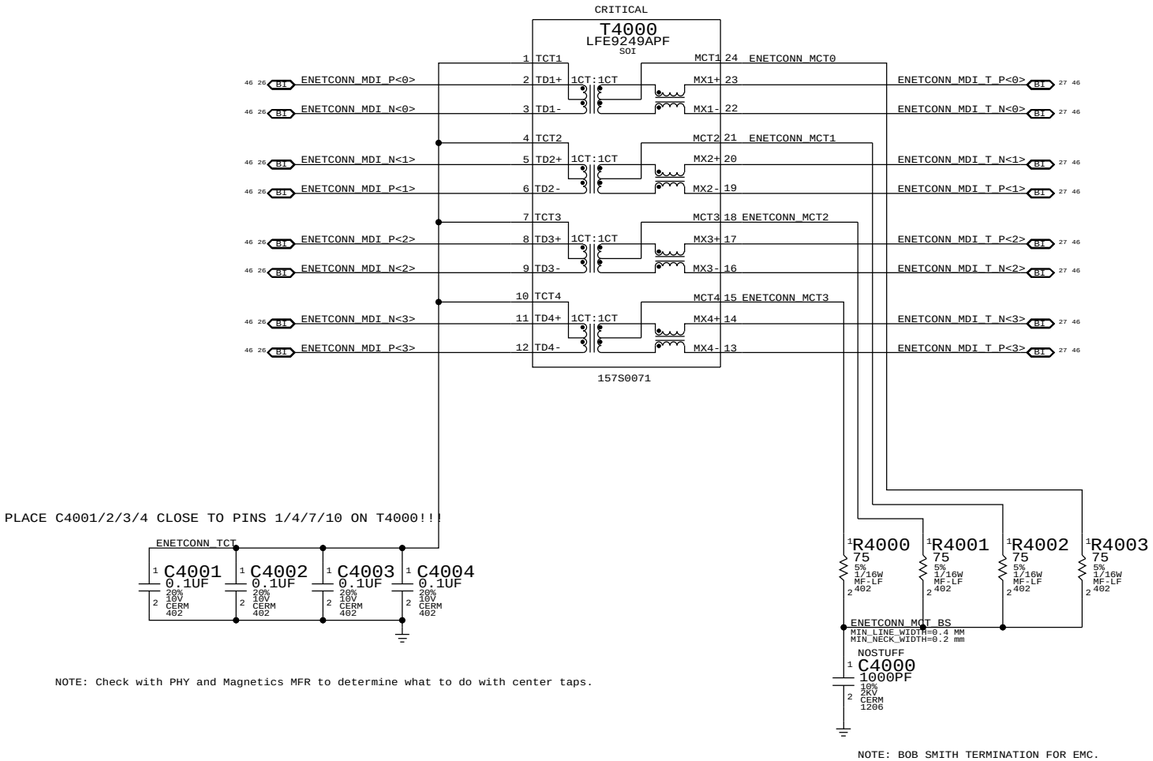
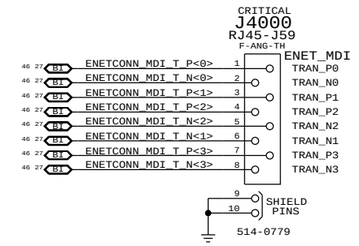
SHEET 26 OF 48





SYNC_MASTER=K62 SYNC_DATE=09/16/2010

PAGE TITLE
Ethernet Connector

Apple Inc.

DRAWING NUMBER 051-8774 SIZE D
REVISION C.0.0
BRANCH
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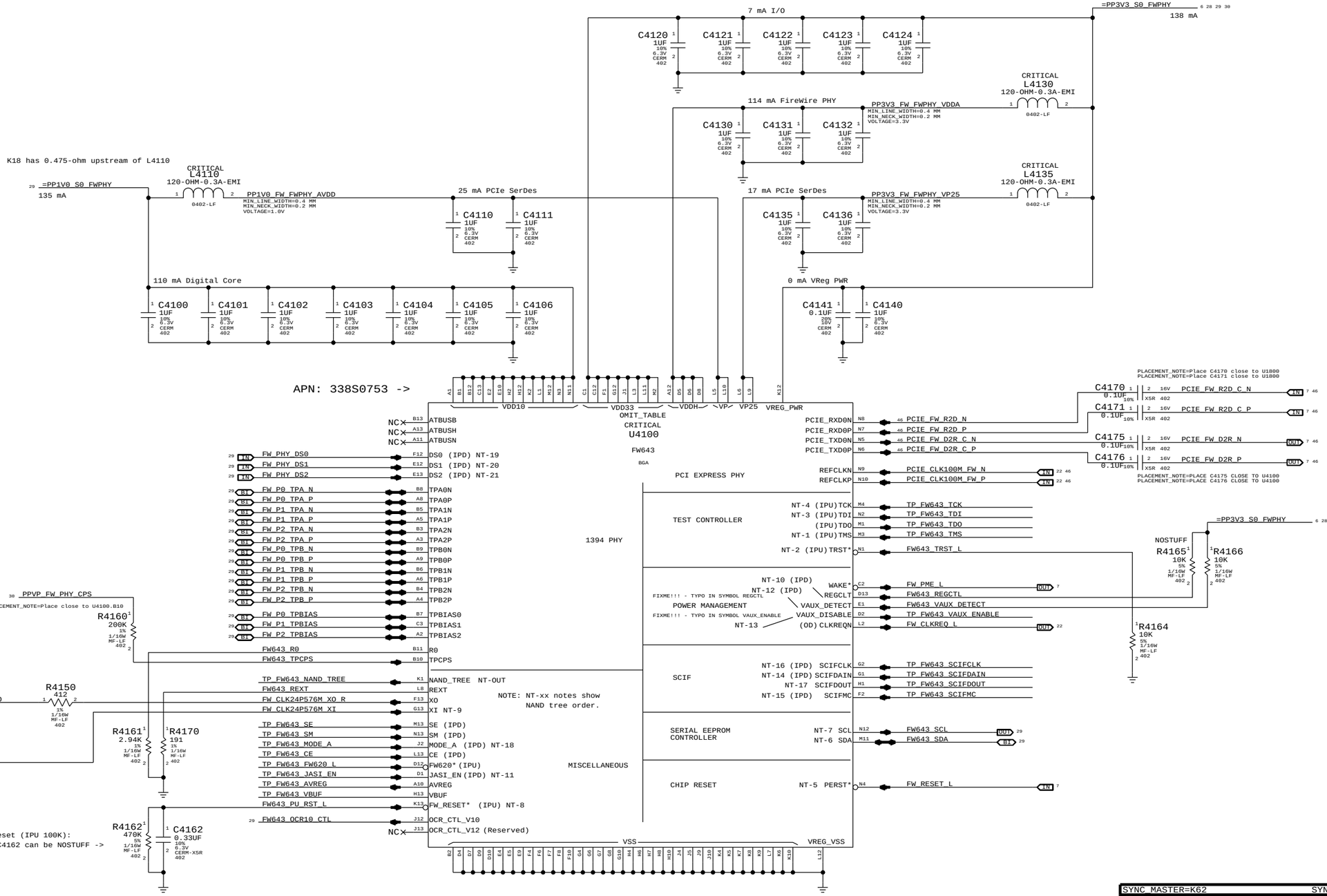
7 mA I/O
=PP3V3_S0_FWPHY
6 28 29 30
138 mA
C4120 1UF 10% 6.3V CERM 402
C4121 1UF 10% 6.3V CERM 402
C4122 1UF 10% 6.3V CERM 402
C4123 1UF 10% 6.3V CERM 402
C4124 1UF 10% 6.3V CERM 402
CRITICAL
L4130
120-OHM-0.3A-EMI
0402-LF
114 mA FireWire PHY
PP3V3_FW_FWPHY_VDDA
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
C4130 1UF 10% 6.3V CERM 402
C4131 1UF 10% 6.3V CERM 402
C4132 1UF 10% 6.3V CERM 402
K18 has 0.475-ohm upstream of L4110
CRITICAL
L4110
120-OHM-0.3A-EMI
=PP1V0_S0_FWPHY
135 mA
PP1V0_FW_FWPHY_AVDD
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.0V
25 mA PCIe SerDes
C4110 1UF 10% 6.3V CERM 402
C4111 1UF 10% 6.3V CERM 402
CRITICAL
L4135
120-OHM-0.3A-EMI
17 mA PCIe SerDes
PP3V3_FW_FWPHY_VP25
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
C4135 1UF 10% 6.3V CERM 402
C4136 1UF 10% 6.3V CERM 402
110 mA Digital Core
C4100 1UF 10% 6.3V CERM 402
C4101 1UF 10% 6.3V CERM 402
C4102 1UF 10% 6.3V CERM 402
C4103 1UF 10% 6.3V CERM 402
C4104 1UF 10% 6.3V CERM 402
C4105 1UF 10% 6.3V CERM 402
C4106 1UF 10% 6.3V CERM 402
0 mA VReg PWR
C4141 0.1UF 20% 10V CERM 402
C4140 1UF 10% 6.3V CERM 402
APN: 338S0753 ->
VDD10
VDD33
VDDH
VP
VP25
VREG_PWR
CRITICAL
U4100
FW643
BGA
PLACEMENT_NOTE=Place C4170 close to U1800
PLACEMENT_NOTE=Place C4171 close to U1800
C4170 0.1UF 10% 16V X5R 402
C4171 0.1UF 10% 16V X5R 402
C4175 0.1UF 10% 16V X5R 402
C4176 0.1UF 10% 16V X5R 402
PLACEMENT_NOTE=PLACE C4175 CLOSE TO U4100
PLACEMENT_NOTE=PLACE C4176 CLOSE TO U4100
PCIE_FW_R2D_C_N
PCIE_FW_R2D_C_P
PCIE_FW_D2R_C_N
PCIE_FW_D2R_C_P
PCIE_RXD0N
PCIE_RXD0P
PCIE_TXD0N
PCIE_TXD0P
REFCLKN
REFCLKP
PCIE_CLK100M_FW_N
PCIE_CLK100M_FW_P
PCI EXPRESS PHY
1394 PHY
TEST CONTROLLER
NT-4 (IPU)TCK
NT-3 (IPU)TDI
(IPU)TDO
NT-1 (IPU)TMS
NT-2 (IPU)TRST*
TP_FW643_TCK
TP_FW643_TDI
TP_FW643_TDO
TP_FW643_TMS
FW643_TRST_L
=PP3V3_S0_FWPHY
6 28 29 30
NOSTUFF
R4165 10K 5% 1/16W MF-LF 402
R4166 10K 5% 1/16W MF-LF 402
R4164 10K 5% 1/16W MF-LF 402
POWER MANAGEMENT
NT-10 (IPD)
NT-12 (IPD)
WAKE*
REGCLT
VAUX_DETECT
VAUX_DISABLE
(OD)CLKREQN
FW_PME_L
FW643_REGCTL
FW643_VAUX_DETECT
TP_FW643_VAUX_ENABLE
FW_CLKREQ_L
FIXME!!! - TYPO IN SYMBOL REGCTL
FIXME!!! - TYPO IN SYMBOL VAUX_ENABLE
NT-13
SCIF
NT-16 (IPD) SCIFCLK
NT-14 (IPD) SCIFDAIN
NT-17 SCIFDOUT
NT-15 (IPD) SCIFMC
TP_FW643_SCIFCLK
TP_FW643_SCIFDAIN
TP_FW643_SCIFDOUT
TP_FW643_SCIFMC
SERIAL EEPROM CONTROLLER
NT-7 SCL
NT-6 SDA
FW643_SCL
FW643_SDA
CHIP RESET
NT-5 PERST*
FW_RESET_L
PPVP_FW_PHY_CPS
PLACEMENT_NOTE=Place close to U4100.B10
R4160 200K 1% 1/16W MF-LF 402
C4150 22PF 5% 50V CERM 402
C4151 22PF 5% 50V CERM 402
FW_CLK24P576M_XO
R4150 412 1% 1/16W MF-LF 402
CRITICAL
Y4150
24.576MHZ
SM-3.2X2.5MM
NC
R4161 2.94K 1% 1/16W MF-LF 402
R4170 191 1% 1/16W MF-LF 402
R4162 470K 5% 1/16W MF-LF 402
C4162 0.33UF 10% 6.3V CERM-X5R 402
External power-on reset (IPU 100K):
Per LSI, R4162 and C4162 can be NOSTUFF ->
FW_PHY_DS0
FW_PHY_DS1
FW_PHY_DS2
FW_P0_TPA_N
FW_P0_TPA_P
FW_P1_TPA_N
FW_P1_TPA_P
FW_P2_TPA_N
FW_P2_TPA_P
FW_P0_TPB_N
FW_P0_TPB_P
FW_P1_TPB_N
FW_P1_TPB_P
FW_P2_TPB_N
FW_P2_TPB_P
FW_P0_TPBIAS
FW_P1_TPBIAS
FW_P2_TPBIAS
FW643_R0
FW643_TPCPS
TP_FW643_NAND_TREE
FW643_REXT
FW_CLK24P576M_XO_R
FW_CLK24P576M_XI
TP_FW643_SE
TP_FW643_SM
TP_FW643_MODE_A
TP_FW643_CE
TP_FW643_FW620_L
TP_FW643_JASI_EN
TP_FW643_AVREG
TP_FW643_VBUF
FW643_PU_RST_L
FW643_OCR10_CTL
ATBUSB
ATBUSH
ATBUSN
DS0 (IPD) NT-19
DS1 (IPD) NT-20
DS2 (IPD) NT-21
TPA0N
TPA0P
TPA1N
TPA1P
TPA2N
TPA2P
TPB0N
TPB0P
TPB1N
TPB1P
TPB2N
TPB2P
TPBIAS0
TPBIAS1
TPBIAS2
R0
TPCPS
NAND_TREE NT-OUT
REXT
XO
XI NT-9
SE (IPD)
SM (IPD)
MODE_A (IPD) NT-18
CE (IPD)
FW620*(IPU)
JASI_EN (IPD) NT-11
AVREG
VBUF
FW_RESET* (IPU) NT-8
OCR_CTL_V10
OCR_CTL_V12 (Reserved)
NOTE: NT-xx notes show NAND tree order.
MISCELLANEOUS
VSS
VREG_VSS
SYNC_MASTER=K62
SYNC_DATE=09/09/2010
PAGE TITLE
FireWire LLC/PHY (FW643)
Apple Inc.
DRAWING NUMBER 051-8774
SIZE D
REVISION C.0.0
BRANCH
PAGE 41 OF 110
SHEET 28 OF 48
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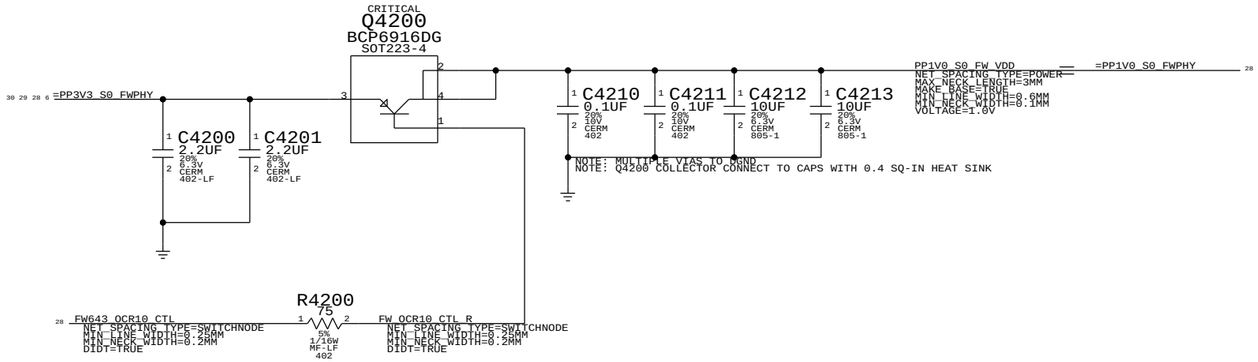
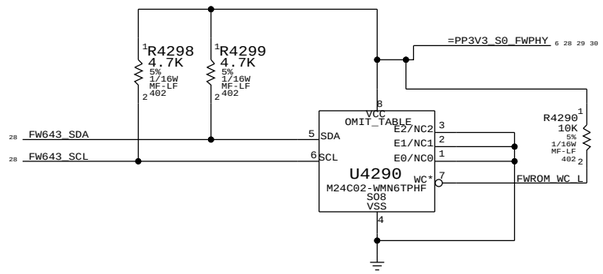
FW643 1.0V GENERATION

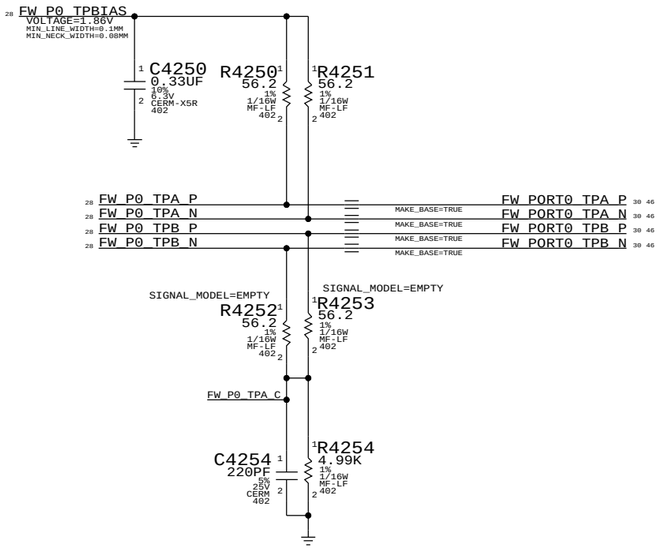


FW643 GUID ROM



Termination

Place close to FireWire PHY



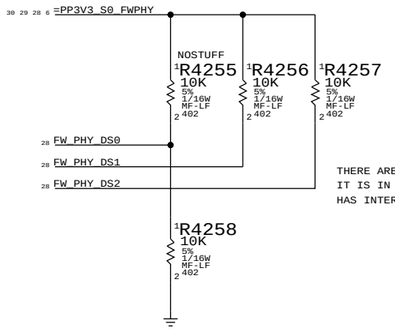
2ND & 3RD TPA/TPB PAIR UNUSED

28 FW_P1_TPBIAS — NC_FW_PORT1_TPBIAS
28 FW_P1_TPA_P — NC_FW_PORT1_TPA_P
28 FW_P1_TPA_N — NC_FW_PORT1_TPA_N
28 FW_P1_TPB_P — NC_FW_PORT1_TPB_P
28 FW_P1_TPB_N — NC_FW_PORT1_TPB_N
28 FW_P2_TPBIAS — NC_FW_PORT2_TPBIAS
28 FW_P2_TPA_P — NC_FW_PORT2_TPA_P
28 FW_P2_TPA_N — NC_FW_PORT2_TPA_N
28 FW_P2_TPB_P — NC_FW_PORT2_TPB_P
28 FW_P2_TPB_N — NC_FW_PORT2_TPB_N

MAKE_BASE=TRUE
NO_TEST=TRUE

NOTE: AGERE'S RECOMMENDATION FOR UNUSED PORTS

1394 PHY DATA/STROBE OPTIONS



THERE ARE THREE FIREWIRE PORTS, BUT ONLY ONE IS USED.NO STUFF MEANS THAT IT IS IN BILINGUL MODE PULL-UPS ASSERT/ENABLE DATA STROBE ONLY MODE, FW643 HAS INTERNAL 100K PULL-DOWNS, ONLY PULL-UPS NECESSARY.

SYNC_MASTER=K62 SYNC_DATE=09/23/2010

PAGE TITLE: FireWire: 1394B MISC

Apple Inc.

DRAWING NUMBER: 051-8774 SIZE: D
REVISION: C.0.0
BRANCH:
PAGE: 42 OF 110
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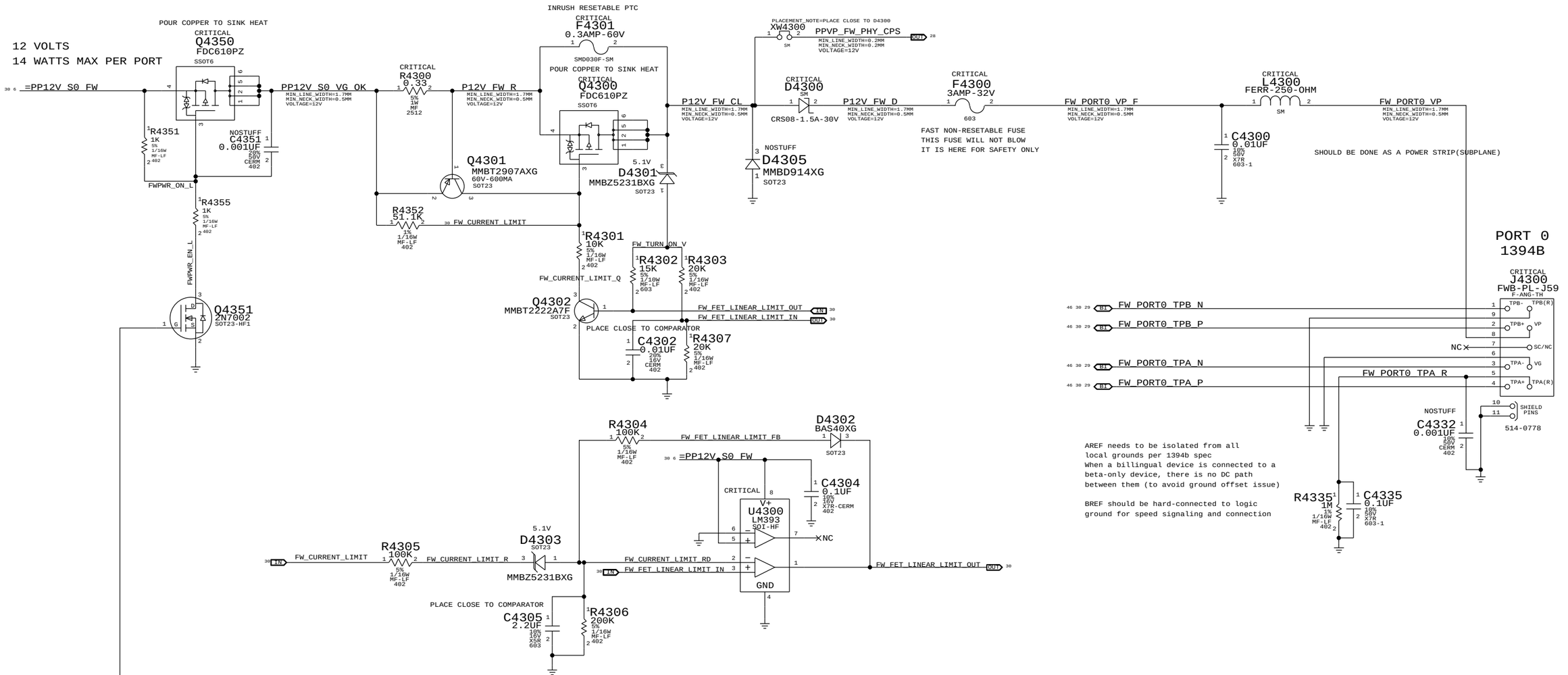

SYNC_MASTER=K62 SYNC_DATE=09/23/2010

PAGE TITLE: FIREWIRE CONNECTOR

Apple Inc.

DRAWING NUMBER: 051-8774 SIZE: D

REVISION: C.0.0

BRANCH:

PAGE: 43 OF 110

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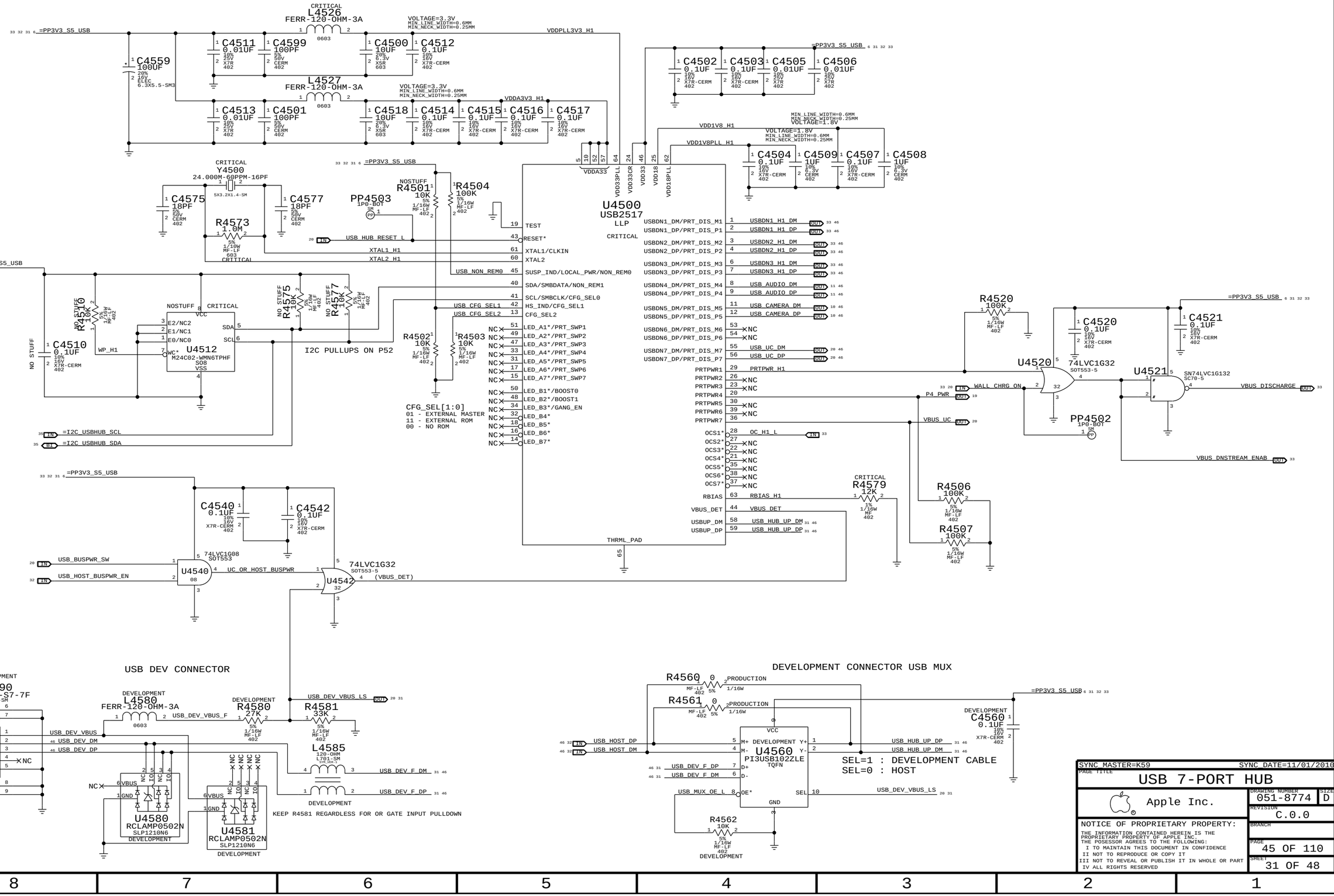

SYNC_MASTER=K59 SYNC_DATE=11/01/2010

PAGE TITLE

USB 7-PORT HUB

Apple Inc.

DRAWING NUMBER 051-8774 SIZE D

REVISION C.0.0

BRANCH

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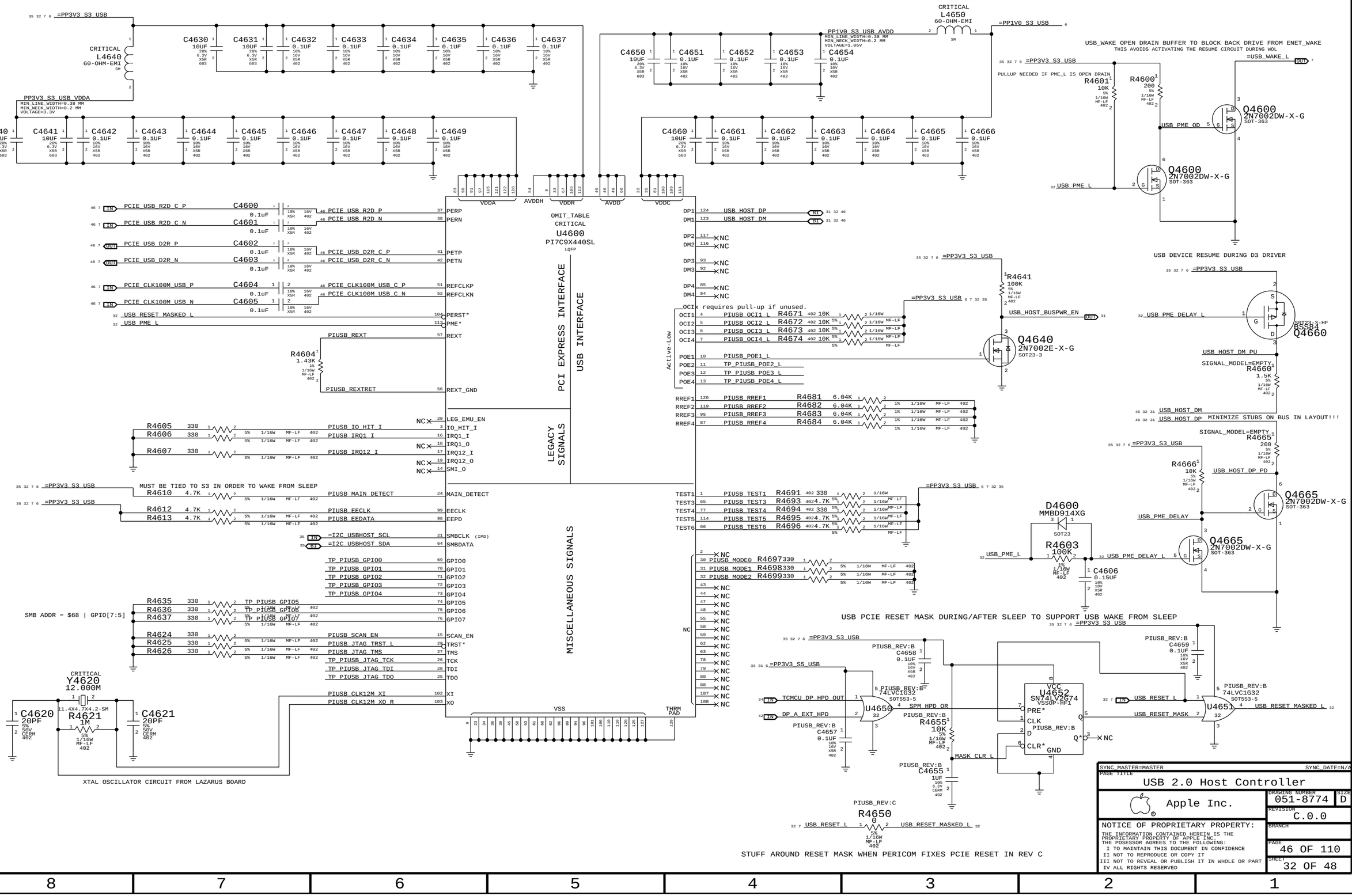
=PP3V3_S3_USB
CRITICAL
L4640
60-OHM-EMI
PP3V3_S3_USB_VDDA
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V
C4630 C4631 C4632 C4633 C4634 C4635 C4636 C4637
C4640 C4641 C4642 C4643 C4644 C4645 C4646 C4647 C4648 C4649
CRITICAL
L4650
60-OHM-EMI
=PP1V0_S3_USB
PP1V0_S3_USB_AVDD
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
C4650 C4651 C4652 C4653 C4654
C4660 C4661 C4662 C4663 C4664 C4665 C4666
VDDA
AVDDH
VDDR
AVDD
VDDC
PCIE_USB_R2D_C_P
PCIE_USB_R2D_C_N
PCIE_USB_D2R_P
PCIE_USB_D2R_N
PCIE_CLK100M_USB_P
PCIE_CLK100M_USB_N
C4600 C4601 C4602 C4603 C4604 C4605
0.1uF
PCIE_USB_R2D_C_P
PCIE_USB_R2D_C_N
PCIE_USB_D2R_C_P
PCIE_USB_D2R_C_N
PCIE_CLK100M_USB_C_P
PCIE_CLK100M_USB_C_N
USB_RESET_MASKED_L
USB_PME_L
PERP
PERN
PETP
PETN
REFCLKP
REFCLKN
PERST*
PME*
PIUSB_REXT
R4604
1.43K
PIUSB_REXTREST
REXT
REXT_GND
OMIT_TABLE
CRITICAL
U4600
PI7C9X440SL
LQFP
PCI EXPRESS INTERFACE
USB INTERFACE
LEGACY SIGNALS
MISCELLANEOUS SIGNALS
DP1
DM1
USB_HOST_DP
USB_HOST_DM
DP2 DM2 DP3 DM3 DP4 DM4
NC
OCIx requires pull-up if unused.
Active-Low
OCI1 OCI2 OCI3 OCI4
PIUSB_OCI1_L
PIUSB_OCI2_L
PIUSB_OCI3_L
PIUSB_OCI4_L
R4671 R4672 R4673 R4674
10K
POE1 POE2 POE3 POE4
TP_PIUSB_POE2_L
TP_PIUSB_POE3_L
TP_PIUSB_POE4_L
RREF1 RREF2 RREF3 RREF4
PIUSB_RREF1
PIUSB_RREF2
PIUSB_RREF3
PIUSB_RREF4
R4681 R4682 R4683 R4684
6.04K
=PP3V3_S3_USB
R4641
100K
USB_HOST_BUSPWR_EN
Q4640
2N7002E-X-G
SOT23-3
USB_WAKE OPEN DRAIN BUFFER TO BLOCK BACK DRIVE FROM ENET_WAKE
THIS AVOIDS ACTIVATING THE RESUME CIRCUIT DURING WOL
=USB_WAKE_L
PULLUP NEEDED IF PME_L IS OPEN DRAIN
R4601
10K
R4600
200
USB_PME_OD
Q4600
2N7002DW-X-G
SOT-363
USB_PME_L
USB DEVICE RESUME DURING D3 DRIVER
USB_PME_DELAY_L
Q4660
BSS84
SOT23-3-HF
USB_HOST_DM_PU
SIGNAL_MODEL=EMPTY
R4660
1.5K
USB_HOST_DM
USB_HOST_DP
MINIMIZE STUBS ON BUS IN LAYOUT!!!
R4665
200
R4666
10K
USB_HOST_DP_PD
Q4665
2N7002DW-X-G
SOT-363
USB_PME_DELAY
D4600
MMBD914XG
SOT23
R4603
100K
C4606
0.15UF
USB_PME_DELAY_L
USB PCIE RESET MASK DURING/AFTER SLEEP TO SUPPORT USB WAKE FROM SLEEP
PIUSB_REV:B
C4658
0.1UF
C4659
0.1UF
C4657
0.1UF
C4655
1UF
U4650
74LVC1G32
SOT553-5
SPM_HPD_OR
U4652
SN74LV2574
VSSOP-HF1
U4651
TCMCU_DP_HPD_OUT
DP_A_EXT_HPD
USB_RESET_L
USB_RESET_MASK
USB_RESET_MASKED_L
MASK_CLR_L
R4655
10K
R4650
0
STUFF AROUND RESET MASK WHEN PERICOM FIXES PCIE RESET IN REV C
MUST BE TIED TO S3 IN ORDER TO WAKE FROM SLEEP
R4610
4.7K
PIUSB_MAIN_DETECT
R4612 R4613
PIUSB_EECLK
PIUSB_EEDATA
=I2C_USBHOST_SCL
=I2C_USBHOST_SDA
SMBCLK (IPD)
SMBDATA
TP_PIUSB_GPIO0
TP_PIUSB_GPIO1
TP_PIUSB_GPIO2
TP_PIUSB_GPIO3
TP_PIUSB_GPIO4
SMB ADDR = $68 | GPIO[7:5]
R4635 R4636 R4637
R4624 R4625 R4626
330
PIUSB_SCAN_EN
PIUSB_JTAG_TRST_L
PIUSB_JTAG_TMS
TP_PIUSB_JTAG_TCK
TP_PIUSB_JTAG_TDI
TP_PIUSB_JTAG_TDO
PIUSB_CLK12M_XI
PIUSB_CLK12M_XO_R
CRITICAL
Y4620
12.000M
11.4X4.7X4.2-SM
C4620 C4621
20PF
R4621
1M
XTAL OSCILLATOR CIRCUIT FROM LAZARUS BOARD
VSS
THRM PAD
TEST1 TEST3 TEST4 TEST5 TEST6
PIUSB_TEST1
PIUSB_TEST3
PIUSB_TEST4
PIUSB_TEST5
PIUSB_TEST6
R4691 R4693 R4694 R4695 R4696
330
4.7K
PIUSB_MODE0
PIUSB_MODE1
PIUSB_MODE2
R4697 R4698 R4699
SYNC_MASTER=MASTER
SYNC_DATE=N/A
PAGE TITLE
USB 2.0 Host Controller
Apple Inc.
DRAWING NUMBER
051-8774
SIZE
D
REVISION
C.0.0
BRANCH
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46 OF 110
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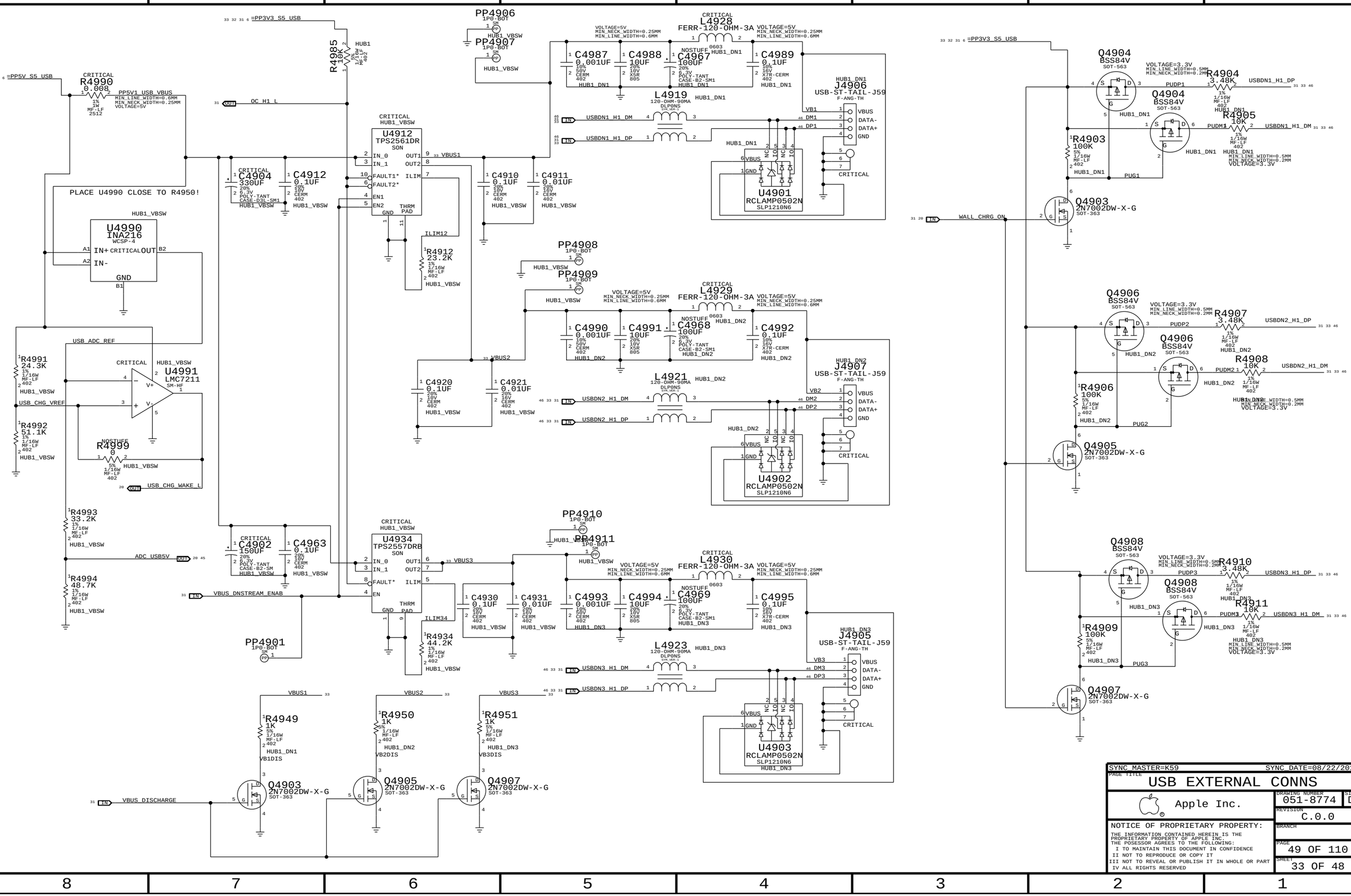
=PP3V3_S5_USB
=PP5V_S5_USB
R4985 10K
HUB1
PP4906 1P0-BOT
PP4907 1P0-BOT
HUB1_VBSW
L4928 FERR-120-OHM-3A
C4987 0.001UF
C4988 10UF
C4967 100UF
C4989 0.1UF
L4919 120-OHM-90MA
J4906 USB-ST-TAIL-J59
R4990 0.008
PP5V1_USB_VBUS
OC_H1_L
U4912 TPS2561DR
C4904 330UF
C4912 0.1UF
C4910 0.1UF
C4911 0.01UF
R4912 23.2K
U4901 RCLAMP0502N
PLACE U4990 CLOSE TO R4950!
U4990 INA216
PP4908 1P0-BOT
PP4909 1P0-BOT
L4929 FERR-120-OHM-3A
C4990 0.001UF
C4991 10UF
C4968 100UF
C4992 0.1UF
L4921 120-OHM-90MA
J4907 USB-ST-TAIL-J59
C4920 0.1UF
C4921 0.01UF
U4902 RCLAMP0502N
USB_ADC_REF
R4991 24.3K
U4991 LMC7211
USB_CHG_VREF
R4992 51.1K
R4999 0
USB_CHG_WAKE_L
R4993 33.2K
R4994 48.7K
ADC_USB5V
C4902 150UF
C4963 0.1UF
U4934 TPS2557DRB
PP4910 1P0-BOT
PP4911 1P0-BOT
L4930 FERR-120-OHM-3A
C4993 0.001UF
C4994 10UF
C4969 100UF
C4995 0.1UF
VBUS_DNSTREAM_ENAB
PP4901 1P0-BOT
R4934 44.2K
L4923 120-OHM-90MA
J4905 USB-ST-TAIL-J59
U4903 RCLAMP0502N
R4949 1K
R4950 1K
R4951 1K
VB1DIS
VB2DIS
VB3DIS
Q4903 2N7002DW-X-G
Q4905 2N7002DW-X-G
Q4907 2N7002DW-X-G
VBUS_DISCHARGE
WALL_CHRG_ON
Q4904 BSS84V
R4904 3.48K
R4905 10K
R4903 100K
Q4903 2N7002DW-X-G
Q4906 BSS84V
R4907 3.48K
R4908 10K
R4906 100K
Q4905 2N7002DW-X-G
Q4908 BSS84V
R4910 3.48K
R4911 10K
R4909 100K
Q4907 2N7002DW-X-G
USBDN1_H1_DP
USBDN1_H1_DM
USBDN2_H1_DP
USBDN2_H1_DM
USBDN3_H1_DP
USBDN3_H1_DM
PUDP1
PUDM1
PUG1
PUDP2
PUDM2
PUG2
PUDP3
PUDM3
PUG3
SYNC_MASTER=K59
SYNC_DATE=08/22/2010
PAGE TITLE
USB EXTERNAL CONNS
Apple Inc.
DRAWING NUMBER 051-8774
SIZE D
REVISION C.0.0
BRANCH
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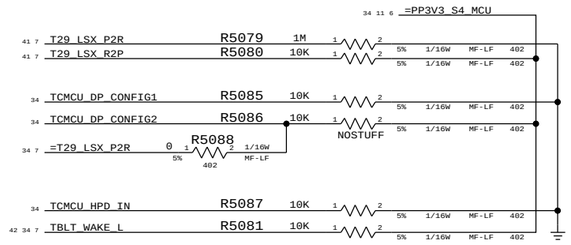
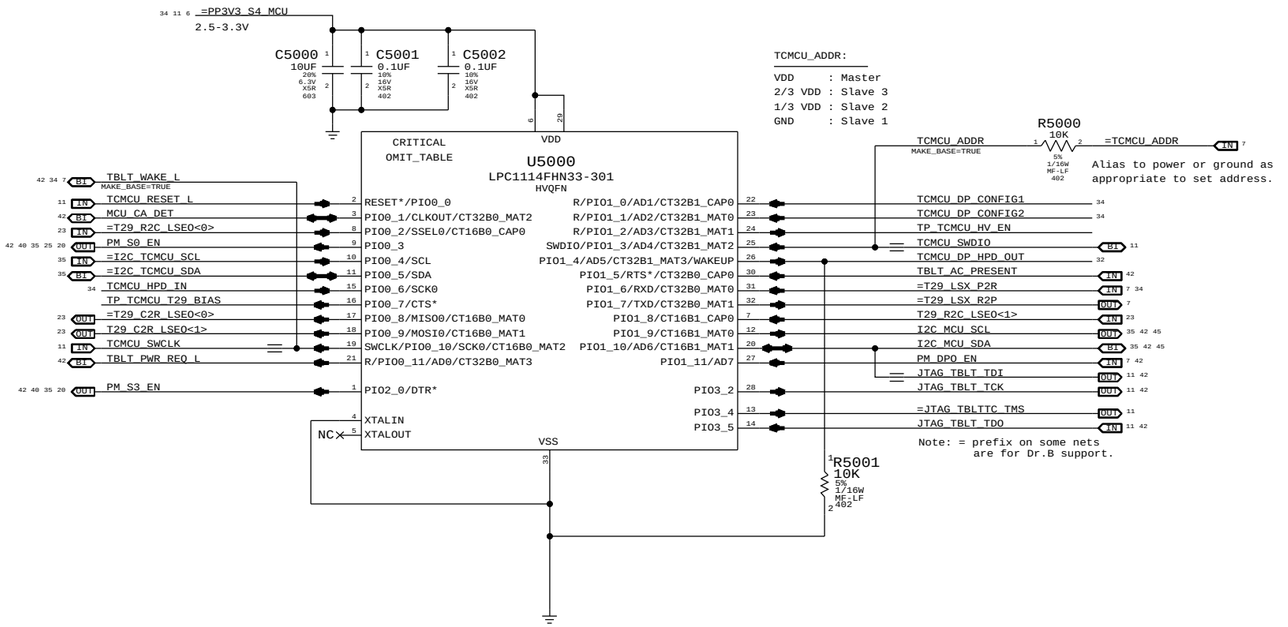
MCU Pull-ups/downs

T29 host/device has 10K pull-up on LSX_R2P.
Dual-plug cable has cross-over for P2R/R2P.

Device micro (U5000) senses pull-up to detect host. Cable may be powered-off until host pull-up is detected.

P2R = Plug to Receptacle
R2P = Receptacle to Plug





SYNC_MASTER=T29_D SYNC_DATE=03/17/2013

PAGE TITLE
Tethered Cable MCU

Apple Inc.

DRAWING NUMBER 051-8774
SIZE D
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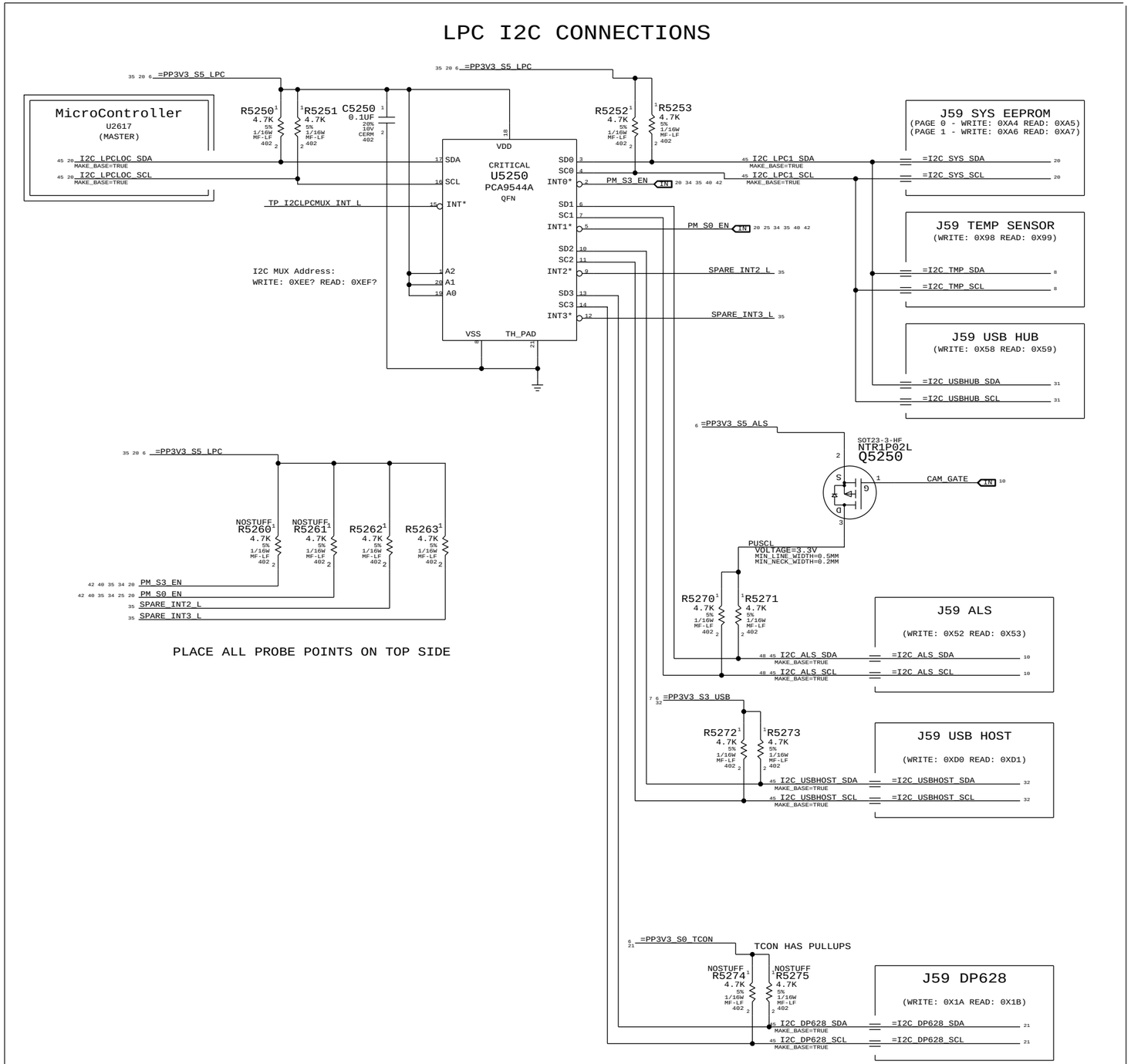
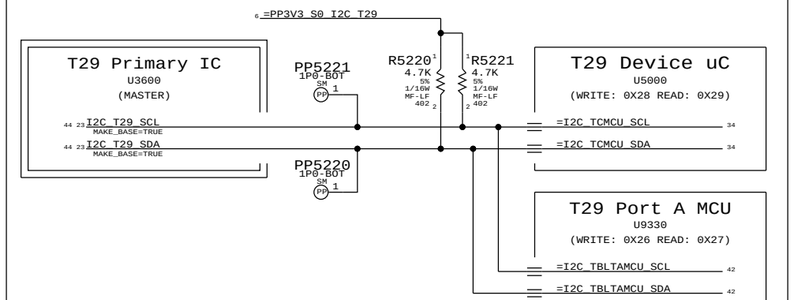
LPC I2C CONNECTIONS



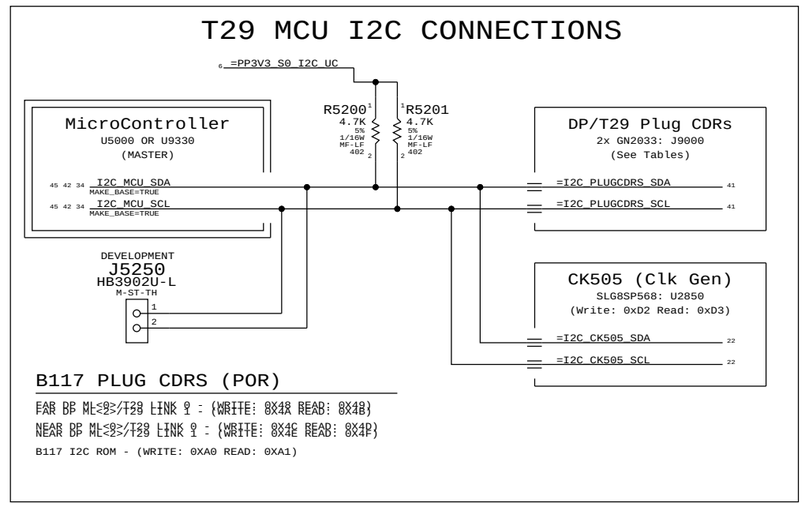
PLACE ALL I2C PROBE POINTS ON TOP SIDE

T29 IC I2C Connections



PLACE ALL I2C PROBE POINTS ON TOP SIDE

T29 MCU I2C CONNECTIONS



B117 PLUG CDRS (POR)

FAR DP ML<0>/T29 LINK 0 - (WRITE: 0X18 READ: 0X19)
NEAR DP ML<0>/T29 LINK 0 - (WRITE: 0X1C READ: 0X1D)
B117 I2C ROM - (WRITE: 0XA0 READ: 0XA1)

SYNC_MASTER=MASTER
SYNC_DATE=N/A

PAGE TITLE
J59 & T29 SMBUS CONNECTIONS

Apple Inc.

DRAWING NUMBER 051-8774
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REVISION C.0.0
BRANCH
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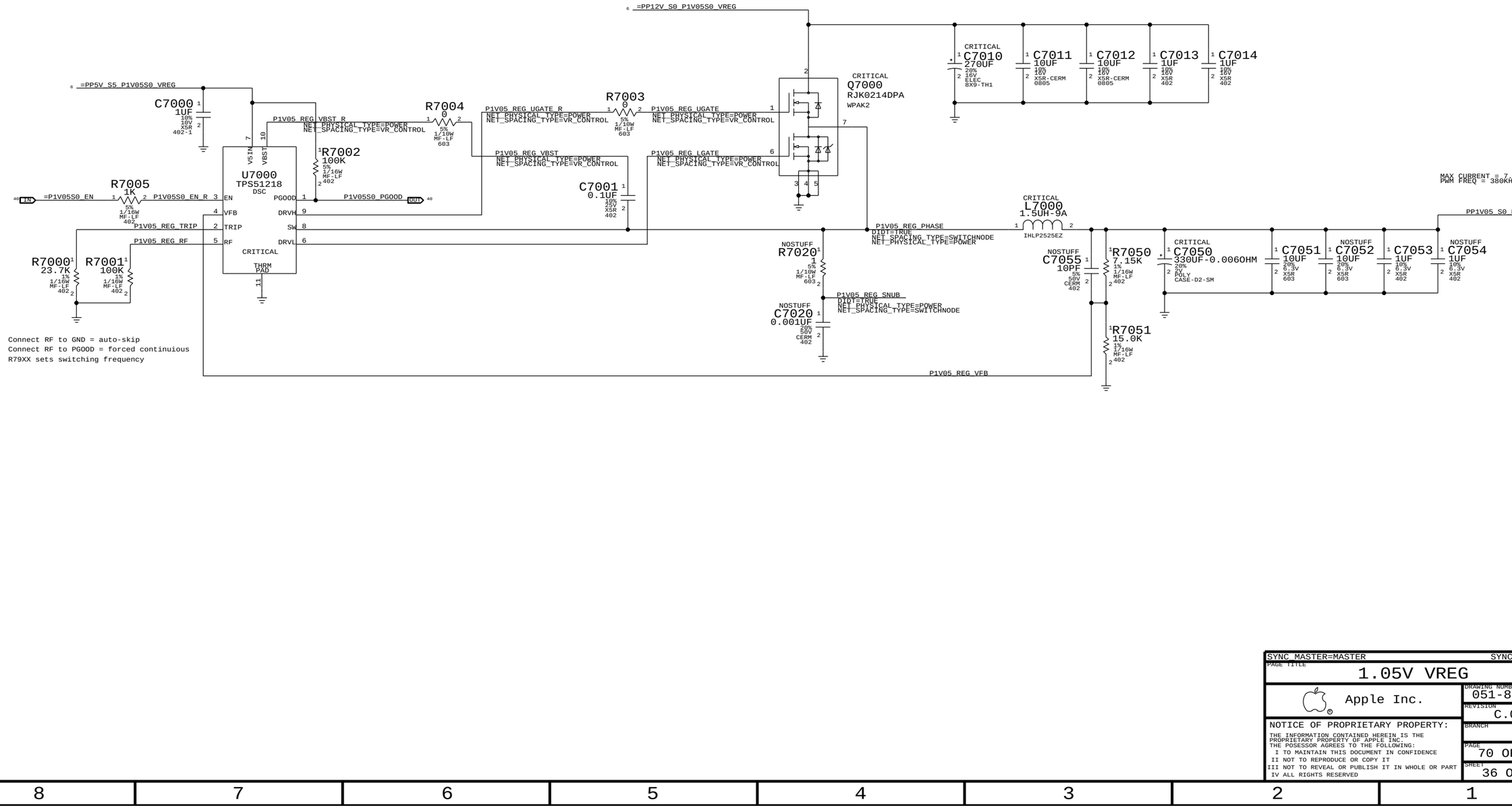

SYNC_MASTER=MASTER SYNC_DATE=N/A

PAGE TITLE

1.05V VREG

Apple Inc.

DRAWING NUMBER 051-8774 SIZE D

REVISION C.0.0

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Page Notes

Power aliases required by this page:
- =PPVIN_SW_T29BST (8-13V Boost Input)
- =PP15V_T29_REG (15V Boost Output)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
T29BST - Stuffs 15V boost regulator

T29 15V Boost Regulator

8-13V Input
Changes required
for 2S.

SI8409DB:
Vds(max): -30V
Vgs(max): +/-12V
Vgs(th): -1.4V
Rds(on): 46mOhm @ 4.5V Vgs
Id(max): 3.7A @ 70C

Voltage not specified here, add property on another page.

UVLO(falling) = 1.22 * (R1 + R2) / R2
UVLO(rising) = UVLO(falling) + (2uA * R1)
UVLO = 4.55V (falling), 4.95 (rising)

SGND shorted to GND inside package, no XW necessary.

Vout = 1.6V * (1 + Ra / Rb)

=PP15V_T29_REG
Vout = 15.47V
Max Current = 1A
Freq = 300KHz

SYNC_MASTER=T29_D	SYNC_DATE=03/17/2011
PAGE TITLE	Power: T29 15V Boost
Apple Inc.	DRAWING NUMBER 051-8774 SIZE D
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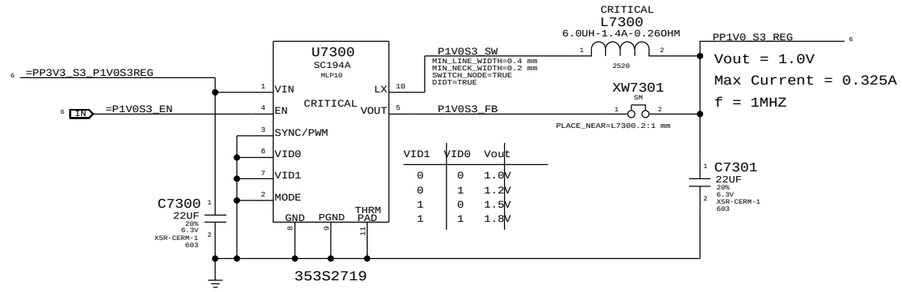
1.0V Switcher



SYNC_MASTER=MASTER SYNC_DATE=N/A

PAGE TITLE

Power: USB (1.0V S3)

Apple Inc.

DRAWING NUMBER 051-8774 SIZE D

REVISION C.0.0

BRANCH

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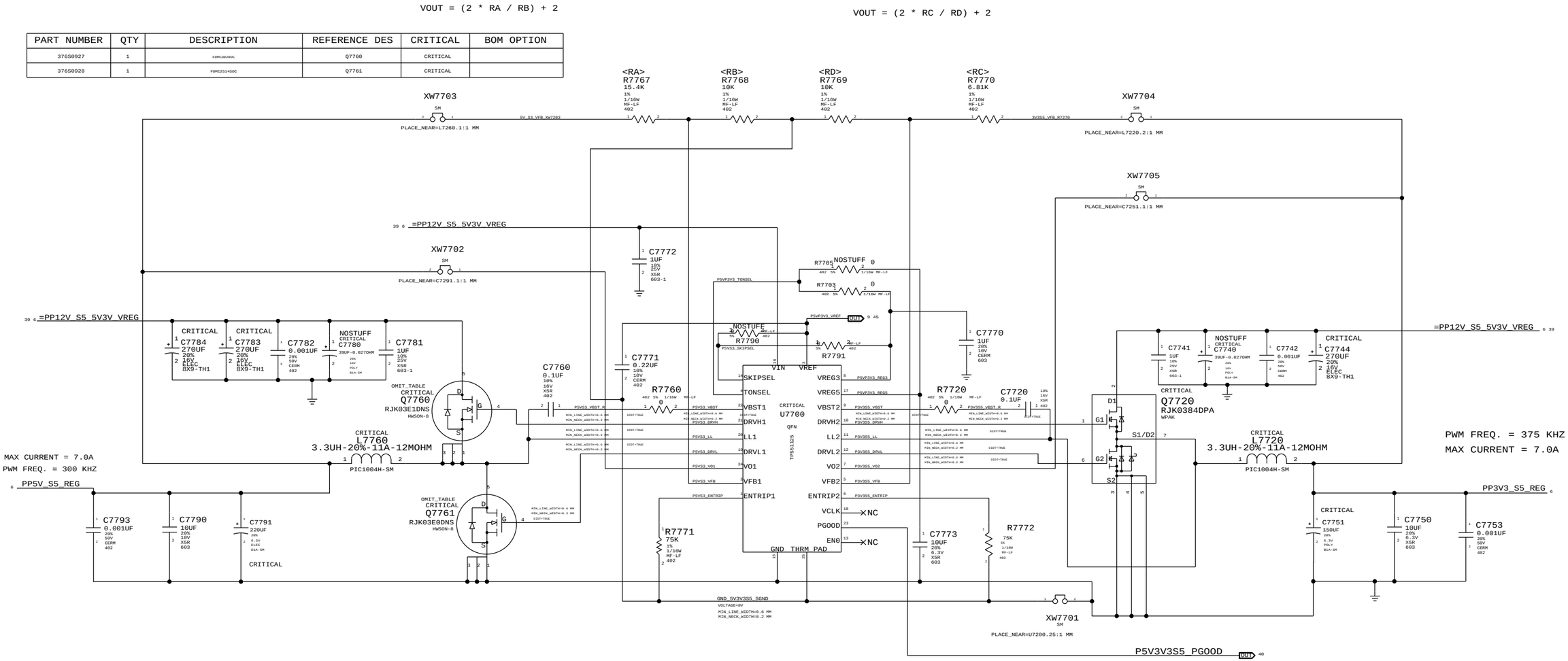
5V_S3/3.3V_S5 POWER SUPPLY

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S0927	1	FDMC3020DC	Q7760	CRITICAL	
376S0928	1	FDMC2514SDC	Q7761	CRITICAL	

VOUT = (2 * RA / RB) + 2

VOUT = (2 * RC / RD) + 2



SYNC_MASTER=MASTER SYNC_DATE=N/A

PAGE TITLE

5V/3.3V SUPPLY

Apple Inc.

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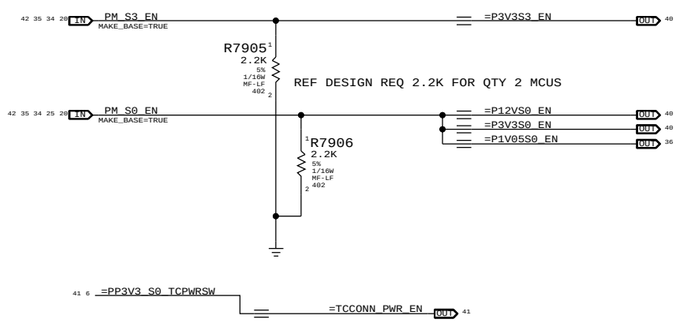
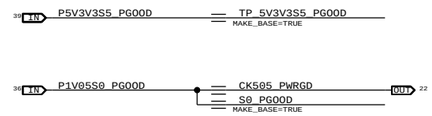
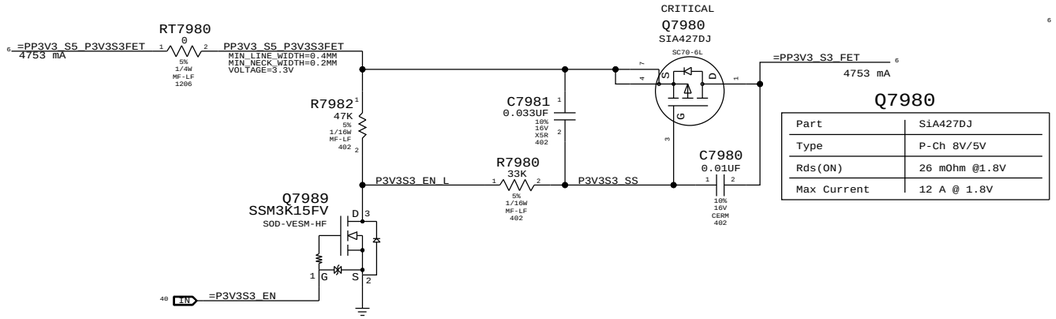
T29 / Device Rails



Power Goods



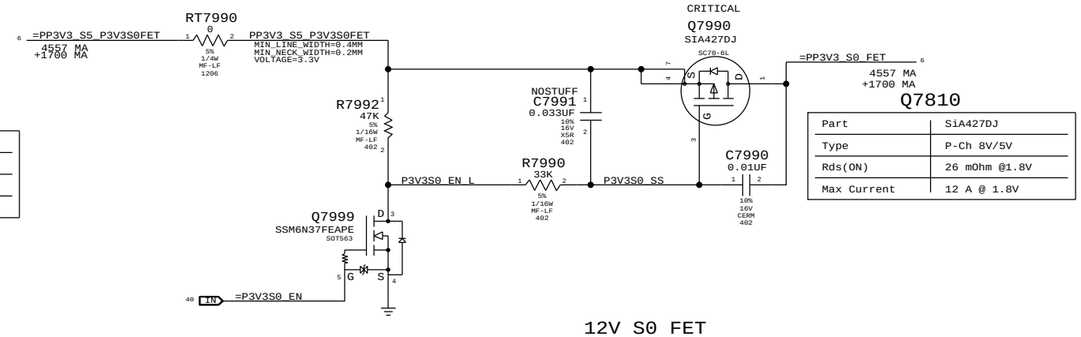
3.3V S3 FET



Q7980

Part	SiA427DJ
Type	P-Ch 8V/5V
Rds(ON)	26 mOhm @1.8V
Max Current	12 A @ 1.8V

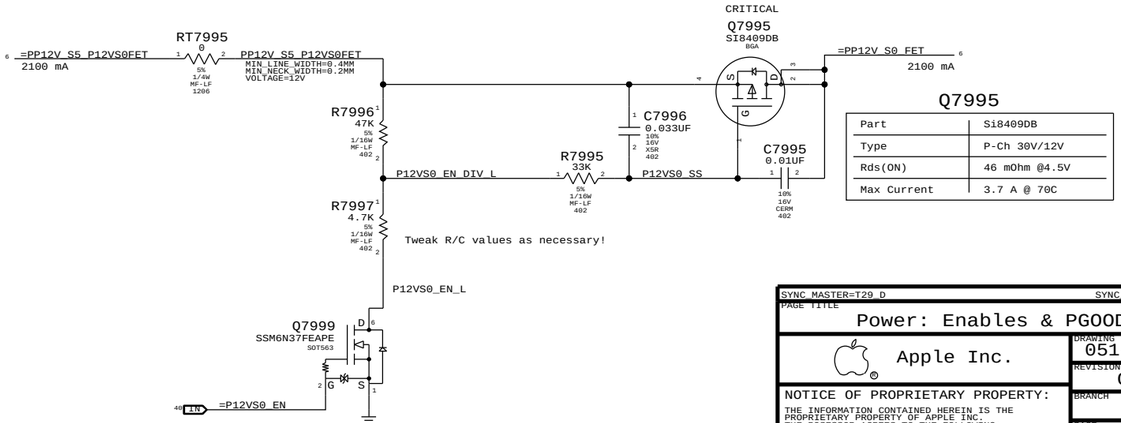
3.3V S0 FET



Q7810

Part	SiA427DJ
Type	P-Ch 8V/5V
Rds(ON)	26 mOhm @1.8V
Max Current	12 A @ 1.8V

12V S0 FET



Q7995

Part	Si8409DB
Type	P-Ch 30V/12V
Rds(ON)	46 mOhm @4.5V
Max Current	3.7 A @ 70C

SYNC_MASTER=T29_D SYNC_DATE=09/30/2010

PAGE TITLE

Power: Enables & PGOODs

Apple Inc.

DRAWING NUMBER 051-8774 SIZE D

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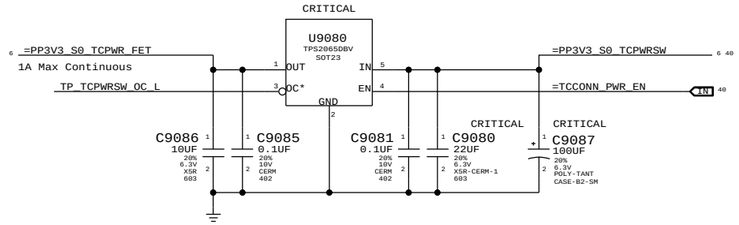
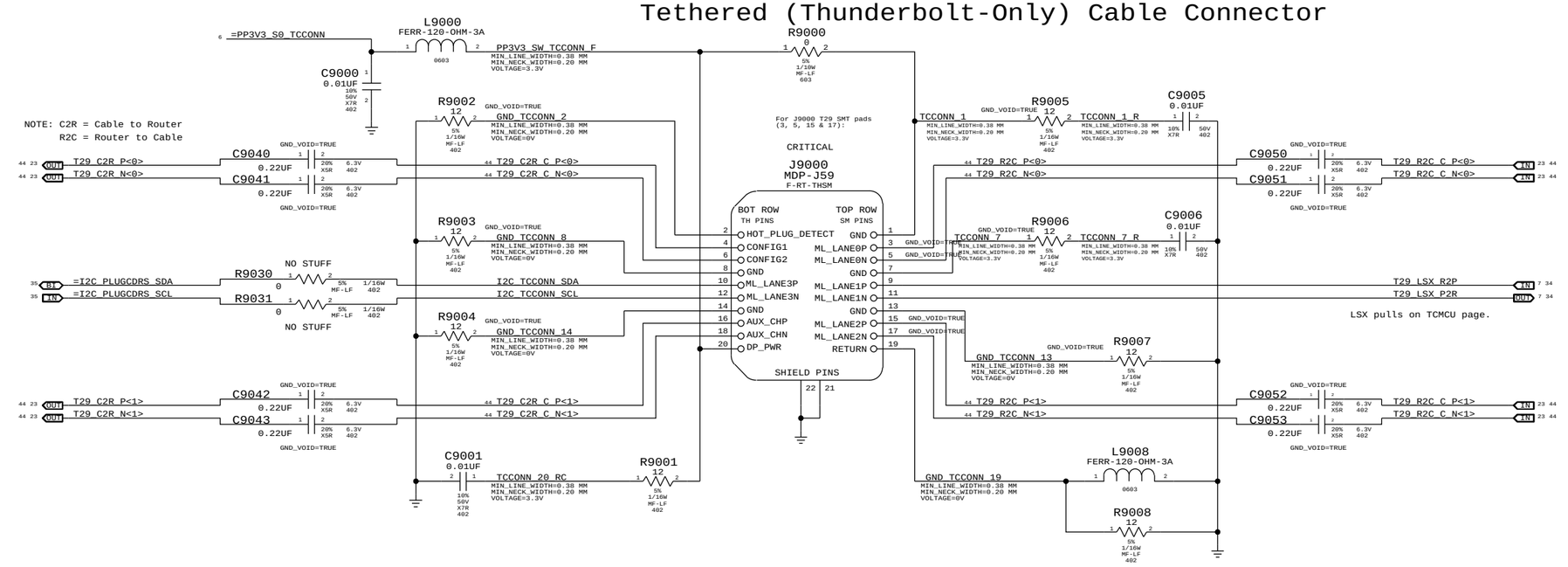
Cable 3.3V Power Switch



Tethered (Thunderbolt-Only) Cable Connector



SYNC_MASTER=T29_D	SYNC_DATE=03/17/2011
PAGE TITLE: Tethered Cable Connector	
Apple Inc.	DRAWING NUMBER: 051-8774 SIZE: D
	REVISION: C.0.0
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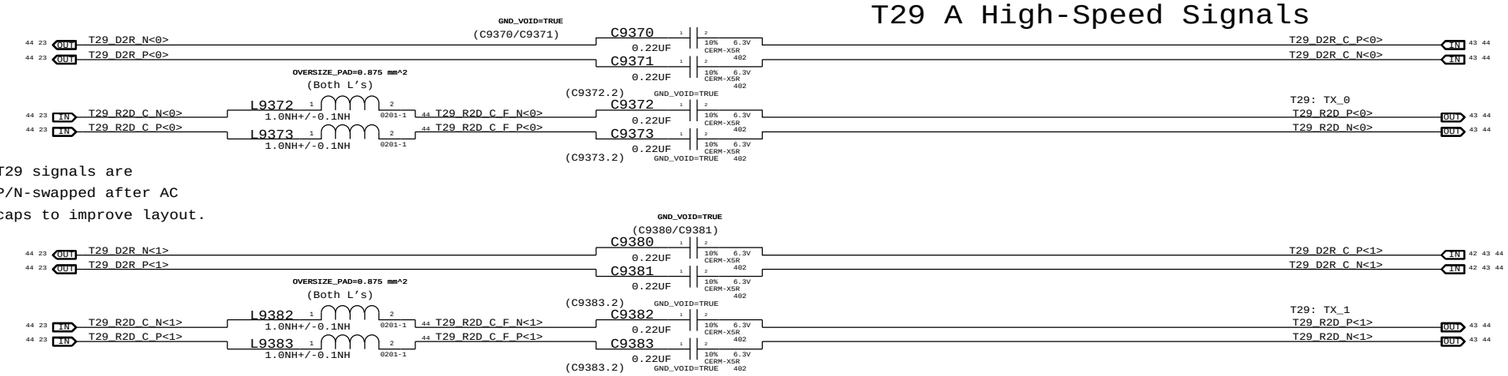
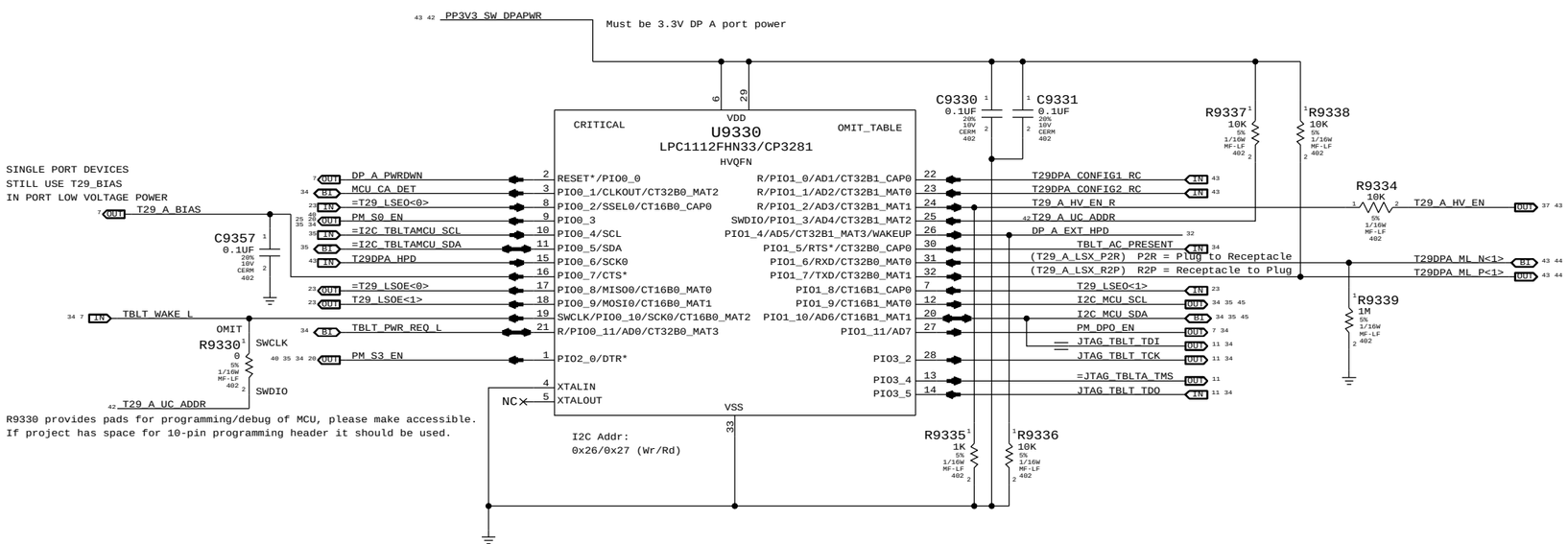
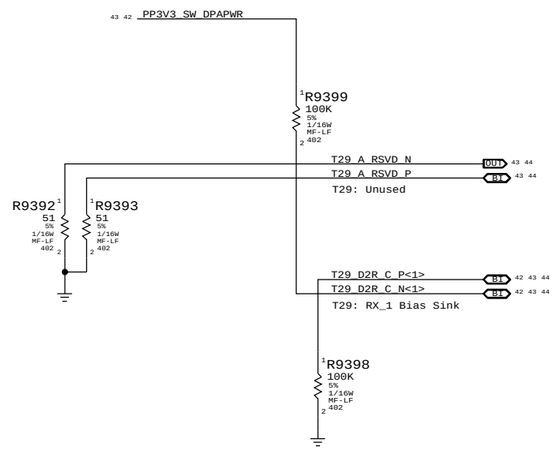
T29 A High-Speed Signals

T29 signals are
P/N-swapped after AC
caps to improve layout.



Port A MCU





SYNC_MASTER=T29_D	SYNC_DATE=11/01/2010
PAGE TITLE	T29 A PORT MICROCONTROLLER
Apple Inc.	DRAWING NUMBER 051-8774 · SIZE D
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Port A HV Power Switch

42 PP3V3_SW_DPAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=3.3V

6 =PPHV_SW_DPAPWRSW
20V Max

R9416 30K 5% 1/16W MF-LF 402

C9410 0.1UF 10% 50V X7R 603-1

U9410 SN1010017 QFN
CRITICAL
VIN VOUT EN* FLT* RTRY* ILIM CT IFLT GND THRM PAD

PPHV_SW_DPAPWR_D
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=15V

DPAPWRSW_HVEN_L
TP_DPAPWRSW_FLT_L
DPAPWRSW_ILIM
DPAPWRSW_IFLT
DPAPWRSW_CT

NOSTUFF R9415 24K 5% 1/16W MF-LF 402
CRITICAL D9415 SOT23 MMBZ5227BLT1H

R9412 0 5% 1/16W MF-LF 402 <CT>

C9411 0.1UF 10% 50V X7R 603-1

R9410 100K 5% 1/16W MF-LF 402 <RFLT>

R9411 210K 1% 1/16W MF-LF 402 <RLIM>

T29HV:P15V

IFLT = 200k / RFLT = 2A
ILIM = 201k / RLIM = 829mA +/- 142mA
TFLT = CCT * 38900
TSD = CCT * 100000

Q9415 SSM3K15FV SOD-VESM-HF

43 42 37 IN T29_A_HV_EN

For 12V systems:
ILIM = 201k / RLIM = 1033mA +/- 156mA

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0434	1	RES,MTL FILM,1/16W,174K,1,0402,SMD,LF	R9411		T29HV:P12V

	Nominal	Min	Max
ILIM	1033mA	877mA	1190mA, tolerance @ 174K per TI

	Nominal	Min	Max
IFLT	2A	1.8A	2.2A
ILIM	829mA	687mA	971mA (*)
TFLT	18.3ms	13.4ms	26.7ms
TSD	470ms	235ms	724ms

(*) U9410 tolerance @ 210K per TI

3.3V/HV Power MUX

3.3V/HV MUXed

R9417 10K 5% 1/16W MF-LF 402

CRITICAL D9410 DSN2 NSR20F20NXXXG

SI8409DB:
Vds(max): -30V
Vgs(max): +/-12V
Vgs(th): -1.4V
Rds(on): 65mOhm @ 2.5V Vgs
Id(max): 3.7A @ 70C

Blocking FET, off when
Source >3.4V or HV_EN high.

CRITICAL D9425 PDMN01-123 DFLS1100

CRITICAL Q9425 SI8409DB 8GA

R9425 4.7K 5% 1/16W MF-LF 402

R9430 4.7K 5% 1/16W MF-LF 402

DPAPWRSW_P3V3_ON_L

Q9427 SSM3K15FV SOD-VESM-HF

Q9426 DMB53D0UV SOT-563

STOP_LEAK

Q9426 DMB53D0UV SOT-563

T29_A_HV_EN 37 42 43

=DPAPWRSW_EN IN 7 43

Bleeder Resistor

2.5V / 249 ohm = 10mA
P = ~27mW

DPAPWR_BLDR_E_R
MIN_LINE_WIDTH=0.20 MM
MIN_NECK_WIDTH=0.20 MM

Q9418 SSM3K15FV SOD-VESM-HF

R9419 249 1% 1/16W MF-LF 402

Q9419 DMB53D0UV SOT-563

DPAPWR_BLDR_E
MIN_LINE_WIDTH=0.20 MM
MIN_NECK_WIDTH=0.20 MM

DPAPWR_BLDR_B

Q9419 DMB53D0UV SOT-563

Note: Bleeder active when T29_A_HV_EN is LOW
and DPAPWRSW_P3V3_ON_L is HIGH (>0.8V).

Port A 3.3V Power Switch

3.3V Always

CRITICAL U9480 TPS2051B SOT23
OUT IN OC* EN GND

DP_PWR must be S4 to support
wake from T29 devices.

=PP3V3_S4_DPAPWRSW 6 7

=DPAPWRSW_EN IN 7 43

C9486 10UF 20% 6.3V X5R 603
C9485 0.1UF 20% 10V CERM 402
C9481 0.1UF 20% 10V CERM 402
C9480 22UF 20% 6.3V X5R-CERM-1 603
C9487 100UF 20% 6.3V POLY-TANT CASE-B2-SM

CRITICAL C9435 0.1UF 20% 10V CERM 402
CRITICAL U9435 ZXRE060A SOT353
IN OUT FB PGND GND

R9435 100K 1% 1/16W MF-LF 402

DPAPWR_FB_DIV

R9436 21.5K 1% 1/16W MF-LF 402

DPAPWRSW_P3V3_ON

L9400 FERR-120-OHM-3A 0603

PP3V3RHV_SW_DPAPWR_UF
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=15V

C9400 0.01UF 10% 50V X7R 402

PP3V3RHV_SW_DPAPWR
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=15V

C9405 0.1UF 10% 25V X5R 402
GND_VOID=TRUE

GND_DPACONN_1
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=0V

DisplayPort/T29 A Connector

DP Dir T29 Dir

CRITICAL J9400 MDP-J59 F-ANG-TH

2	HPD	GND	1
4	CONFIG1	ML_LANE0P	3
6	CONFIG2	ML_LANE0N	5
8	GND	GND	7
10	ML_LANE3P	ML_LANE1P	9
12	ML_LANE3N	ML_LANE1N	11
14	GND	GND	13
16	AUX_CHP	ML_LANE2P	15
18	AUX_CHN	ML_LANE2N	17
20	DP_PWR	RETURN	19

SHIELD PINS 22 21

T29: TX_0

GND_DPACONN_7
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=0V

C9406 0.1UF 10% 25V X5R 402

GND_DPACONN_13
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=0V

R9407 12 5% 1/16W MF-LF 402

T29: TX_1

GND_DPACONN_19
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=0V

L9408 FERR-120-OHM-3A 0603

R9408 12 5% 1/16W MF-LF 402

R9470 470K 5% 1/20W MF 201
R9471 470K 5% 1/20W MF 201
R9472 470K 5% 1/20W MF 201
R9473 470K 5% 1/20W MF 201

470k R's for ESD protection
on AC-coupled signals.

T29_D2R_C_P<0> IN 42 44
T29_D2R_C_N<0> IN 42 44
T29_D2R_C_P<1> IN 42 44
T29_D2R_C_N<1> IN 42 44

T29DPA_ML_P<1> IN 42 44
T29DPA_ML_N<1> IN 42 44

T29: LSX_R2P/P2R (P/N)

R9403 12 5% 1/16W MF-LF 402
R9404 12 5% 1/16W MF-LF 402
GND_DPACONN_8
GND_DPACONN_14
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=0V

T29_A_RSVD_P
T29_A_RSVD_N
T29: Unused

R9402 12 5% 1/16W MF-LF 402
T29DPA_HPD_R

R9401 12 5% 1/16W MF-LF 402
DPACONN_20_RC
MIN_LINE_WIDTH=0.38 MM
MIN_NECK_WIDTH=0.20 MM
VOLTAGE=16V

C9402 0.01UF 10% 50V X7R 402
C9401 0.01UF 10% 50V X7R 402

R9494 1K 5% 1/16W MF-LF 402 SIGNAL_MODEL=EMPTY
R9495 1K 5% 1/16W MF-LF 402 SIGNAL_MODEL=EMPTY

T29DPA_HPD
T29DPA_CONFIG1_RC
T29DPA_CONFIG2_RC

R9452 1M 5% 1/16W MF-LF 402
R9451 1M 5% 1/16W MF-LF 402

C9494 330PF 10% 50V CERM 402
C9495 330PF 10% 50V CERM 402

DP Source must pull
down HPD input with
greater than or equal
to 100K (DPv1.1a).

Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

R9441 100K 5% 1/16W MF-LF 402

SYNC_MASTER=MASTER SYNC_DATE=N/A
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DisplayPort/T29 A Connector

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PCI-Express Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
PCIEG2_85D	*	N	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
PCIEG2_85D	TOP,BOTTOM	Y	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
PCIEG2	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?
PCIEG2	TOP,BOTTOM	=4X_DIELECTRIC	?

T29 I2C Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
I2C_55SE	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	0.1MM	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
I2C	*	=2x_DIELECTRIC	?

T29 SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_SPI	*	=2x_DIELECTRIC	?

T29/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29DP_90D	*	N	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
T29DP_90D	TOP,BOTTOM	Y	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	*	=5x_DIELECTRIC	?

SOURCE: Bill Cornelius's T29 Routing Notes

DP CONNECTOR SIGNAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=4:1_SPACING	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4:1_SPACING	?

T29 Net Properties

T29 DP AND DOWNSTREAM PORTS

T29/DP TETHERED CABLE

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
PCIE_CLK100M_T29	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_T29_P	22 23
PCIE_CLK100M_T29	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_T29_N	22 23
	I2C_55SE	I2C	I2C_T29_SCL	23 35
	I2C_55SE	I2C	I2C_T29_SDA	23 35
T29_SPI_CLK	T29_SPI_55S	T29_SPI	T29_SPI_CLK	23
T29_SPI_MOSI	T29_SPI_55S	T29_SPI	T29_SPI_MOSI	23
T29_SPI_MISO	T29_SPI_55S	T29_SPI	T29_SPI_MISO	23
T29_SPI_CS_L	T29_SPI_55S	T29_SPI	T29_SPI_CS_L	23
	T29DP_90D	T29DP	T29_R2D_C_P<3..0>	23 42
	T29DP_90D	T29DP	T29_R2D_C_N<3..0> BEAD_PROBE=TRUE	23 42
	T29DP_90D	T29DP	T29_D2R_P<3..0> BEAD_PROBE=TRUE	23 42
	T29DP_90D	T29DP	T29_D2R_N<3..0> BEAD_PROBE=TRUE	23 42
T29_R2D0	T29DP_90D	T29DP	T29_R2D_P<0> BEAD_PROBE=TRUE	42 43
T29_R2D0	T29DP_90D	T29DP	T29_R2D_N<0> BEAD_PROBE=TRUE	42 43
T29_R2D1	T29DP_90D	T29DP	T29_R2D_P<1> BEAD_PROBE=TRUE	42 43
T29_R2D1	T29DP_90D	T29DP	T29_R2D_N<1> BEAD_PROBE=TRUE	42 43
	T29DP_90D	T29DP	T29_R2D_C_F_P<1..0> BEAD_PROBE=TRUE	42
	T29DP_90D	T29DP	T29_R2D_C_F_N<1..0> BEAD_PROBE=TRUE	42
T29_D2R0	T29DP_90D	T29DP	T29_D2R_C_P<0> BEAD_PROBE=TRUE	42 43
T29_D2R0	T29DP_90D	T29DP	T29_D2R_C_N<0> BEAD_PROBE=TRUE	42 43
T29_D2R1	T29DP_90D	T29DP	T29_D2R_C_P<1> BEAD_PROBE=TRUE	42 43
T29_D2R1	T29DP_90D	T29DP	T29_D2R_C_N<1> BEAD_PROBE=TRUE	42 43
	DP_90D	DISPLAYPORT	T29DPA_ML_P<1>	42 43
	DP_90D	DISPLAYPORT	T29DPA_ML_N<1>	42 43
	USB2_90D	USB2	T29_A_RSVD_P	42 43
	USB2_90D	USB2	T29_A_RSVD_N	42 43
	T29DP_90D	T29DP	T29_R2C_P<1..0> BEAD_PROBE=TRUE	41
	T29DP_90D	T29DP	T29_R2C_N<1..0> BEAD_PROBE=TRUE	41
T29_R2C0	T29DP_90D	T29DP	T29_R2C_C_P<0> BEAD_PROBE=TRUE	23 41
T29_R2C0	T29DP_90D	T29DP	T29_R2C_C_N<0> BEAD_PROBE=TRUE	23 41
T29_R2C1	T29DP_90D	T29DP	T29_R2C_C_P<1> BEAD_PROBE=TRUE	23 41
T29_R2C1	T29DP_90D	T29DP	T29_R2C_C_N<1> BEAD_PROBE=TRUE	23 41
T29_C2R0	T29DP_90D	T29DP	T29_C2R_P<0> BEAD_PROBE=TRUE	23 41
T29_C2R0	T29DP_90D	T29DP	T29_C2R_N<0> BEAD_PROBE=TRUE	23 41
T29_C2R1	T29DP_90D	T29DP	T29_C2R_P<1> BEAD_PROBE=TRUE	23 41
T29_C2R1	T29DP_90D	T29DP	T29_C2R_N<1> BEAD_PROBE=TRUE	23 41
	T29DP_90D	T29DP	T29_C2R_C_P<1..0> BEAD_PROBE=TRUE	41
	T29DP_90D	T29DP	T29_C2R_C_N<1..0> BEAD_PROBE=TRUE	41

INTERNAL PANEL PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
R360	DP_90D	DISPLAYPORT	DP_INT_ML_C_P<3..0>	7
R367	DP_90D	DISPLAYPORT	DP_INT_ML_C_N<3..0>	7
R368 DP_INT_ML	DP_90D	DISPLAYPORT	DP_INT_ML_P<3..0>	7 21 48
R369 DP_INT_ML	DP_90D	DISPLAYPORT	DP_INT_ML_N<3..0>	7 21 48
R371	DP_90D	DISPLAYPORT	DP_INT_AUXCH_C_P	7
R374	DP_90D	DISPLAYPORT	DP_INT_AUXCH_C_N	7
R372 DP_INT_AUXCH	DP_90D	DISPLAYPORT	DP_INT_AUXCH_P	7 21 48
R373 DP_INT_AUXCH	DP_90D	DISPLAYPORT	DP_INT_AUXCH_N	7 21 48

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Temp Sensor Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TMPSNS_PAIR	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	20MM	0.25MM	0.10MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TMPSNS	*	=2x_DIELECTRIC	?

Temp Sensor Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
I42A	TMPSNS_PAIR	TMPSNS	DX1_P	8
I42B	TMPSNS_PAIR	TMPSNS	DX1_N	8
I43A	TMPSNS_PAIR	TMPSNS	TDX1_P	8 48
I42C	TMPSNS_PAIR	TMPSNS	TDX1_N	8 48
I42D	TMPSNS_PAIR	TMPSNS	DX2_P	8
I43B	TMPSNS_PAIR	TMPSNS	DX2_N	8
I43D	TMPSNS_PAIR	TMPSNS	TDX2_P	8 48
I42E	TMPSNS_PAIR	TMPSNS	TDX2_N	8 48

Temp sensor routes

AUDIO CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUDIODIFF	*	Y	0.6 MM	0.2 MM	10 MM	0.2 MM	0.2 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
AUDIO	*	0.2 MM	?

AUDIO NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
I448	AUDIODIFF	AUDIO	AUD_LTWT_N	15
I449	AUDIODIFF	AUDIO	AUD_LTWT_P	15
I450	AUDIODIFF	AUDIO	AUD_LWFR_N	15
I451	AUDIODIFF	AUDIO	AUD_LWFR_P	15
I452	AUDIODIFF	AUDIO	AUD_RTWT_N	16
I453	AUDIODIFF	AUDIO	AUD_RTWT_P	16
I454	AUDIODIFF	AUDIO	AUD_RWFR_N	16
I455	AUDIODIFF	AUDIO	AUD_RWFR_P	16
I456	AUDIODIFF	AUDIO	AUD_SUB_N	17
I457	AUDIODIFF	AUDIO	AUD_SUB_P	17

SPEAKER NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
I458	AUDIODIFF	AUDIO	SPKRAMP_LTWT_OUT_N	15 18 48
I459	AUDIODIFF	AUDIO	SPKRAMP_LTWT_OUT_P	15 18 48
I460	AUDIODIFF	AUDIO	SPKRAMP_LWFR_OUT_N	15 18 48
I461	AUDIODIFF	AUDIO	SPKRAMP_LWFR_OUT_P	15 18 48
I462	AUDIODIFF	AUDIO	SPKRAMP_RTWT_OUT_N	16 18 48
I463	AUDIODIFF	AUDIO	SPKRAMP_RTWT_OUT_P	16 18 48
I464	AUDIODIFF	AUDIO	SPKRAMP_RWFR_OUT_N	16 18 48
I465	AUDIODIFF	AUDIO	SPKRAMP_RWFR_OUT_P	16 18 48
I466	AUDIODIFF	AUDIO	SPKRAMP_SUB_OUT_N	17 18 48
I467	AUDIODIFF	AUDIO	SPKRAMP_SUB_OUT_P	17 18 48

I2C Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	I2C_5SSE	I2C	I2C_LPCREM_SDA	20 21
	I2C_5SSE	I2C	I2C_LPCREM_SCL	20 21
	I2C_5SSE	I2C	DDC_SDA_FC	21 48
	I2C_5SSE	I2C	DDC_SCL_FC	21 48
	I2C_5SSE	I2C	SDA_FC	21 48
	I2C_5SSE	I2C	SCL_FC	21 48
	I2C_5SSE	I2C	SDA_SWREM	21
	I2C_5SSE	I2C	SCL_SWREM	21
	I2C_5SSE	I2C	I2C_DP628_SDA	35
	I2C_5SSE	I2C	I2C_DP628_SCL	35
	I2C_5SSE	I2C	I2C_LPCLOC_SDA	20 35
	I2C_5SSE	I2C	I2C_LPCLOC_SCL	20 35
	I2C_5SSE	I2C	I2C_FALS_SDA	10
	I2C_5SSE	I2C	I2C_FALS_SCL	10
	I2C_5SSE	I2C	I2C_LPC1_SDA	35
	I2C_5SSE	I2C	I2C_LPC1_SCL	35
	I2C_5SSE	I2C	I2C_ALS_SCL	35 48
	I2C_5SSE	I2C	I2C_ALS_SDA	35 48
	I2C_5SSE	I2C	I2C_USBHOST_SCL	35
	I2C_5SSE	I2C	I2C_USBHOST_SDA	35

I2C pairs from LPC

	I2C_5SSE	I2C	ADAV4601_I2C_SDA	14
	I2C_5SSE	I2C	ADAV4601_I2C_SCL	14
	I2C_5SSE	I2C	I2C_SDA	12 14 18
	I2C_5SSE	I2C	I2C_SCL	12 14 18
	I2C_5SSE	I2C	AUD_161_I2C_SDA	12
	I2C_5SSE	I2C	AUD_161_I2C_SCL	12

Audio I2C pairs

	I2C_5SSE	I2C	I2C_MCU_SCL	34 35 42
	I2C_5SSE	I2C	I2C_MCU_SDA	34 35 42

MicroCtlr Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	MICROCTLR_5SSE	MICROCTLR	ADC_STR0_V	9 20
	MICROCTLR_5SSE	MICROCTLR	ADC_STR1_V	9 20
	MICROCTLR_5SSE	MICROCTLR	ADC_STR2_V	9 20
	MICROCTLR_5SSE	MICROCTLR	DAC_OUT	9 20
	MICROCTLR_5SSE	MICROCTLR	ADC_USB5V	20 33
	MICROCTLR_5SSE	MICROCTLR	P5VP3V3_VREF	9 39

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Ethernet MDI Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_MDI_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	25 MIL	?

SOURCE: MCP73 Interface DG (DG-02974-001_v01), Section 2.7.4

PCIe Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
H17	PCIE_85D	PCIE	PCIE_ENET_R2D_P 26
H18	PCIE_85D	PCIE	PCIE_ENET_R2D_N 26
H19 PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET_R2D_C_P 7 26
H20 PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET_R2D_C_N 7 26
H21 PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET_D2R_P 7 26
H22 PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET_D2R_N 7 26
H23	PCIE_85D	PCIE	PCIE_ENET_D2R_C_P 26
H24	PCIE_85D	PCIE	PCIE_ENET_D2R_C_N 26
H25 PCIE_CLK100M_ENET	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_P 22 26
H26 PCIE_CLK100M_ENET	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_N 22 26

Ethernet MDI Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
H25 ENET_MDI	ENET_MDI_100D	ENET_MDI	ENETCONN_MDI_P<3..0> 26 27
H27 ENET_MDI	ENET_MDI_100D	ENET_MDI	ENETCONN_MDI_N<3..0> 26 27
H19	ENET_MDI_100D	ENET_MDI	ENETCONN_MDI_T_P<3..0> 27
H20	ENET_MDI_100D	ENET_MDI	ENETCONN_MDI_T_N<3..0> 27

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

FIREWIRE PCIE NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
	PCIE_85D	PCIE	PCIE_FW_R2D_P 28
	PCIE_85D	PCIE	PCIE_FW_R2D_N 28
PCIE_FW_R2D	PCIE_85D	PCIE	PCIE_FW_R2D_C_P 7 28
PCIE_FW_R2D	PCIE_85D	PCIE	PCIE_FW_R2D_C_N 7 28
PCIE_FW_D2R	PCIE_85D	PCIE	PCIE_FW_D2R_P 7 28
PCIE_FW_D2R	PCIE_85D	PCIE	PCIE_FW_D2R_N 7 28
	PCIE_85D	PCIE	PCIE_FW_D2R_C_P 28
	PCIE_85D	PCIE	PCIE_FW_D2R_C_N 28
PCIE_CLK100M_FW	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_P 22 28
PCIE_CLK100M_FW	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_N 22 28

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
FW_P0_TPA	FW_110D	FW_TP	FW_PORT0_TPA_P 29 30
FW_P0_TPA	FW_110D	FW_TP	FW_PORT0_TPA_N 29 30
FW_P0_TPB	FW_110D	FW_TP	FW_PORT0_TPB_P 29 30
FW_P0_TPB	FW_110D	FW_TP	FW_PORT0_TPB_N 29 30

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB2_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB2	*	=4:1_SPACING	?

USB PCIE NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
	PCIEG2_85D	PCIEG2	PCIE_USB_D2R_C_P 32
	PCIEG2_85D	PCIEG2	PCIE_USB_D2R_C_N 32
	PCIEG2_85D	PCIEG2	PCIE_USB_R2D_P 32
	PCIEG2_85D	PCIEG2	PCIE_USB_R2D_N 32
PCIE_USB_R2D	PCIEG2_85D	PCIEG2	PCIE_USB_R2D_C_P 7 32
PCIE_USB_R2D	PCIEG2_85D	PCIEG2	PCIE_USB_R2D_C_N 7 32
PCIE_USB_D2R	PCIEG2_85D	PCIEG2	PCIE_USB_D2R_P 7 32
PCIE_USB_D2R	PCIEG2_85D	PCIEG2	PCIE_USB_D2R_N 7 32
PCIE_CLK100M_USB	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_USB_P 7 32
PCIE_CLK100M_USB	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_USB_N 7 32
PCIE_CLK100M_USB	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_USB_C_P 32
PCIE_CLK100M_USB	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_USB_C_N 32

USB Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
USB UPSTREAM		USB2_90D	USB2	USB_HUB_UP_DP 31
		USB2_90D	USB2	USB_HUB_UP_DM 31
		USB2_90D	USB2	USB_DEV_DP 31
		USB2_90D	USB2	USB_DEV_DM 31
		USB2_90D	USB2	USB_DEV_F_DP 31
		USB2_90D	USB2	USB_DEV_F_DM 31
		USB2_90D	USB2	USB_HOST_DP 31 32
		USB2_90D	USB2	USB_HOST_DM 31 32
USB Hub ports		USB2_90D	USB2	USBDN1_H1_DP 31 33
		USB2_90D	USB2	USBDN1_H1_DM 31 33
		USB2_90D	USB2	USBDN2_H1_DP 31 33
		USB2_90D	USB2	USBDN2_H1_DM 31 33
		USB2_90D	USB2	USBDN3_H1_DP 31 33
		USB2_90D	USB2	USBDN3_H1_DM 31 33
		USB2_90D	USB2	USB_UC_DP 20 31
		USB2_90D	USB2	USB_UC_DM 20 31
		USB2_90D	USB2	USB_AUDIO_DP 11 31
		USB2_90D	USB2	USB_AUDIO_DM 11 31
		USB2_90D	USB2	USB_CAMERA_DP 10 31
		USB2_90D	USB2	USB_CAMERA_DM 10 31
		USB2_90D	USB2	CAM_DP 10 48
		USB2_90D	USB2	CAM_DM 10 48
USB AUDIO		USB2_90D	USB2	AUD_161_USB_DP 12
		USB2_90D	USB2	AUD_161_USB_DM 12
USB connector routes		USB2_90D	USB2	DM1 33
		USB2_90D	USB2	DP1 33
		USB2_90D	USB2	DM2 33
		USB2_90D	USB2	DP2 33
		USB2_90D	USB2	DM3 33
		USB2_90D	USB2	DP3 33

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T29 Dr.B-Specific Physical & Spacing Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,BOTTOM	NO_TYPE	MM	15.7

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=55_OHM_SE	=55_OHM_SE	6.35 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD
55_OHM_SE	TOP,BOTTOM	Y	0.085 MM	0.085 MM			

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3,ISL6	Y	0.120 MM	0.120 MM		0.150 MM	0.150 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.135 MM	0.135 MM		0.160 MM	0.160 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL6	Y	0.115 MM	0.115 MM		0.200 MM	0.200 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.125 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL6	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.099 MM	0.099 MM		0.150 MM	0.150 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL6	Y	0.081 MM	0.081 MM		0.250 MM	0.250 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.091 MM	0.091 MM		0.250 MM	0.250 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL6	Y	0.067 MM	0.067 MM		0.300 MM	0.300 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.075 MM	0.075 MM		0.300 MM	0.300 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

Standard Spacing Rules

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	*	0.1 MM	?
2:1_SPACING	*	0.2 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?
5:1_SPACING	*	0.5 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	TOP,BOTTOM	0.140 MM	?
3X_DIELECTRIC	TOP,BOTTOM	0.210 MM	?
4X_DIELECTRIC	TOP,BOTTOM	0.280 MM	?
5X_DIELECTRIC	TOP,BOTTOM	0.355 MM	?
2X_DIELECTRIC	*	0.152 MM	?
3X_DIELECTRIC	*	0.228 MM	?
4X_DIELECTRIC	*	0.304 MM	?
5X_DIELECTRIC	*	0.380 MM	?

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FUNCTIONAL TEST POINTS

J1013 ODD FAN

8 IN FAN0_PWR FUNC_TEST=TRUE
8 IN FAN_TACH0 FUNC_TEST=TRUE
19 IN PP12V_FAN_FET FUNC_TEST=TRUE
MIN_ALLOWED_TPS=3

3 GROUND TESTPOINTS NEAR J1013

J1115 BLC CONNECTOR

9 IN STR0_+ FUNC_TEST=TRUE
9 IN STR0_- FUNC_TEST=TRUE
9 IN STR0C FUNC_TEST=TRUE
9 IN STR1_+ FUNC_TEST=TRUE
9 IN STR1_- FUNC_TEST=TRUE
9 IN STR1C FUNC_TEST=TRUE
9 IN STR2_+ FUNC_TEST=TRUE
9 IN STR2_- FUNC_TEST=TRUE
9 IN STR2C FUNC_TEST=TRUE

2 GROUND TESTPOINTS NEAR J1013

J1204 USB CAMERA

10 IN PP5V_CAM_FILT FUNC_TEST=TRUE
MIN_ALLOWED_TPS=1
46 10 IN CAM_DM FUNC_TEST=TRUE
46 10 IN CAM_DP FUNC_TEST=TRUE
45 35 IN I2C_ALS_SCL FUNC_TEST=TRUE
45 35 IN I2C_ALS_SDA FUNC_TEST=TRUE

4 GROUND TESTPOINTS NEAR J1204

J2007 MICROPHONE

18 IN AUD_MIC_IN_N_CONN FUNC_TEST=TRUE
18 IN GND_AUD_MIC_CONN FUNC_TEST=TRUE
18 IN AUD_MIC_IN_P_CONN FUNC_TEST=TRUE

2 GROUND TESTPOINTS NEAR J2007

J2003 AUDIO LEFT SPEAKER

45 18 19 IN SPKRAMP_LWFR_OUT_P FUNC_TEST=TRUE
45 18 19 IN SPKRAMP_LWFR_OUT_N FUNC_TEST=TRUE
45 18 19 IN SPKRAMP_LTWT_OUT_P FUNC_TEST=TRUE
45 18 19 IN SPKRAMP_LTWT_OUT_N FUNC_TEST=TRUE

J2004 AUDIO RIGHT SPEAKER

45 18 16 IN SPKRAMP_RWFR_OUT_P FUNC_TEST=TRUE
45 18 16 IN SPKRAMP_RWFR_OUT_N FUNC_TEST=TRUE
45 18 16 IN SPKRAMP_RTWT_OUT_P FUNC_TEST=TRUE
45 18 16 IN SPKRAMP_RTWT_OUT_N FUNC_TEST=TRUE

J2005 AUDIO SUBWOOFER

45 18 17 IN SPKRAMP_SUB_OUT_P FUNC_TEST=TRUE
45 18 17 IN SPKRAMP_SUB_OUT_N FUNC_TEST=TRUE
18 17 16 15 13 IN GND_AUDIO_SPKRAMP FUNC_TEST=TRUE
MIN_ALLOWED_TPS=6

J1011 BLOWER TEMP SENSOR

45 8 IN TDX1_N FUNC_TEST=TRUE
45 8 IN TDX1_P FUNC_TEST=TRUE

2 GROUND TESTPOINTS NEAR J1011

J1012 PSU TEMP SENSOR

45 8 IN TDX2_N FUNC_TEST=TRUE
45 8 IN TDX2_P FUNC_TEST=TRUE

2 GROUND TESTPOINTS NEAR J1012

J2726 PANEL POWER

21 IN PP12V_PANEL_FC FUNC_TEST=TRUE
MIN_ALLOWED_TPS=4

4 GROUND TESTPOINTS NEAR J2726

J2725 INTERNAL DP PANEL

44 21 7 IN DP_INT_ML_P<3..0> FUNC_TEST=TRUE
44 21 7 IN DP_INT_ML_N<3..0> FUNC_TEST=TRUE
44 21 7 IN DP_INT_AUXCH_P FUNC_TEST=TRUE
44 21 7 IN DP_INT_AUXCH_N FUNC_TEST=TRUE
45 21 IN DDC_SCL_FC FUNC_TEST=TRUE
45 21 IN DDC_SDA_FC FUNC_TEST=TRUE
45 21 IN SCL_FC FUNC_TEST=TRUE
45 21 IN SDA_FC FUNC_TEST=TRUE
21 IN AUDIO_ON_FC FUNC_TEST=TRUE
21 IN AUDIO_MUTE_FC_L FUNC_TEST=TRUE
21 IN I2S_SCLK_FC FUNC_TEST=TRUE
21 IN I2S_WS_FC FUNC_TEST=TRUE
21 IN I2S_SD0_FC FUNC_TEST=TRUE
21 IN DP_PWR_UP_FC FUNC_TEST=TRUE
21 IN INT_FC_L FUNC_TEST=TRUE
21 IN DP_INT_HPD_FC FUNC_TEST=TRUE
21 IN VIDEO_ON_FC FUNC_TEST=TRUE
21 IN VSYNC_FC FUNC_TEST=TRUE

17 GROUND TESTPOINTS NEAR J2725

GND 36 TP'S FUNC_TEST=TRUE
MIN_ALLOWED_TPS=36

NC AND NO_TEST NETS

FLIP SIDE PCI BRIDGE AND USB CONTROLLER MOUNTING AND ROUTING MAKES TEST VIRTUALLY IMPOSSIBLE

TP_PCIBR_WAKE_L = NC_PCIBR_WAKE_L MAKE_BASE=TRUE NO_TEST=TRUE
TP_PEX8112_EECS_L = NC_PEX8112_EECS_L MAKE_BASE=TRUE NO_TEST=TRUE
TP_PEX8112_EECLK = NC_PEX8112_EECLK MAKE_BASE=TRUE NO_TEST=TRUE
TP_PEX8112_EERDDATA = NC_PEX8112_EERDDATA MAKE_BASE=TRUE NO_TEST=TRUE
TP_PEX8112_EEWRDATA = NC_PEX8112_EEWRDATA MAKE_BASE=TRUE NO_TEST=TRUE
TP_PEX8112_GPIO0 = NC_PEX8112_GPIO0 MAKE_BASE=TRUE NO_TEST=TRUE
TP_PEX8112_GPIO1 = NC_PEX8112_GPIO1 MAKE_BASE=TRUE NO_TEST=TRUE
TP_PEX8112_GPIO2 = NC_PEX8112_GPIO2 MAKE_BASE=TRUE NO_TEST=TRUE
TP_PEX8112_GPIO3 = NC_PEX8112_GPIO3 MAKE_BASE=TRUE NO_TEST=TRUE
TP_PEX8112_PWR_OK = NC_PEX8112_PWR_OK MAKE_BASE=TRUE NO_TEST=TRUE
TP_PEX8112_BAR0ENB_L = NC_PEX8112_BAR0ENB_L MAKE_BASE=TRUE NO_TEST=TRUE
TP_PEX8112_PCLKO62SEL_L = NC_PEX8112_PCLKO62SEL_L MAKE_BASE=TRUE NO_TEST=TRUE
TP_PEX8112_PMEOUT_L = NC_PEX8112_PMEOUT_L MAKE_BASE=TRUE NO_TEST=TRUE
TP_PEX8112_GNT1_L = NC_PEX8112_GNT1_L MAKE_BASE=TRUE NO_TEST=TRUE
TP_PEX8112_GNT2_L = NC_PEX8112_GNT2_L MAKE_BASE=TRUE NO_TEST=TRUE
TP_PEX8112_GNT3_L = NC_PEX8112_GNT3_L MAKE_BASE=TRUE NO_TEST=TRUE
TP_PEX8112_PCLKO = NC_PEX8112_PCLK0 MAKE_BASE=TRUE NO_TEST=TRUE

TP_NECUSB_SMI_L = NC_NECUSB_SMI_L MAKE_BASE=TRUE NO_TEST=TRUE
TP_NECUSB_PPON1 = NC_NECUSB_PPON1 MAKE_BASE=TRUE NO_TEST=TRUE
TP_NECUSB_PPON2 = NC_NECUSB_PPON2 MAKE_BASE=TRUE NO_TEST=TRUE
TP_NECUSB_PPON3 = NC_NECUSB_PPON3 MAKE_BASE=TRUE NO_TEST=TRUE
TP_NECUSB_SRCLK = NC_NECUSB_SRCLK MAKE_BASE=TRUE NO_TEST=TRUE
TP_NECUSB_SRDTA = NC_NECUSB_SRDTA MAKE_BASE=TRUE NO_TEST=TRUE
TP_NECUSB_SRMOD = NC_NECUSB_SRMOD MAKE_BASE=TRUE NO_TEST=TRUE
TP_NECUSB_TESTEN = NC_NECUSB_TESTEN MAKE_BASE=TRUE NO_TEST=TRUE
TP_NECUSB_TEST3 = NC_NECUSB_TEST3 MAKE_BASE=TRUE NO_TEST=TRUE
TP_NECUSB_TEST4 = NC_NECUSB_TEST4 MAKE_BASE=TRUE NO_TEST=TRUE

PCI_AD<31..0> NO_TEST=TRUE
PCI_C_BE_L<3..0> NO_TEST=TRUE
PCI_PAR NO_TEST=TRUE
PCI_FRAME_L NO_TEST=TRUE
PCI_IRDY_L NO_TEST=TRUE
PCI_TRDY_L NO_TEST=TRUE
PCI_DEVSEL_L NO_TEST=TRUE
PCI_STOP_L NO_TEST=TRUE
PCI_PERR_L NO_TEST=TRUE
PCI_SERR_L NO_TEST=TRUE
PCI_NECUSB_REQ_L NO_TEST=TRUE
PCI_NECUSB_GNT_L NO_TEST=TRUE
PCI_NECUSB_INT_L NO_TEST=TRUE
PCI_CLKRUN_L NO_TEST=TRUE
PCI_RESET_L NO_TEST=TRUE

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